

64000

**HP64000
Logic Development
System**

**Model 64622A
40 Channel State
Acquisition Board**



**HEWLETT
PACKARD**

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SERVICE MANUAL

MODEL 64622A 40 CHANNEL STATE ACQUISITION BOARD

REPAIR NUMBERS

This manual applies to 64622A 40 Channel State Acquisition Boards with a repair number prefix of 2144A. For further information on repair numbers refer to "Instruments Covered by This Manual" in Section I, and Section VII for Backdating to earlier Models.

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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Figure 1-1. Model 64622A 40 Channel Acquisition Board

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual contains information required to install, test and service the Hewlett-Packard Model 64622A 40 Channel State Acquisition Board (40 Ch ACQ). Operating instructions are provided in a separate Operating Manual supplied with the instrument. It should be kept with the instrument for use by the operator.

1-3. SPECIFICATIONS.

1-4. Normally instrument specifications are listed in this section. However, the Model 64622A Acquisition Board cannot function without a Model 64621A State Analysis Control Board, and for the purpose of the State Analysis Subsystem Specifications the two models are considered as one unit. Therefore, the specifications are listed only in the Model 64621A State Analysis Control Board Service Manual, Section I, General Information.

1-5. INSTRUMENTS COVERED BY THIS MANUAL.

1-6. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-7. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual for the newer instrument.

1-8. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-9. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Office.

1-10. RECOMMENDED TEST EQUIPMENT.

1-11. Equipment required to maintain the Model 64622A is listed in Table 1-1. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-1. Recommended Test Equipment

4 1/2 Digit Multimeter with +/-1 mV accuracy.....	HP 3466A
Signature Multimeter.....	HP 5005A

1-12. DESCRIPTION.

1-13. The State Analyzer is used to monitor information flow in the data domain. The information may be a software program, the actions of a hardware state machine, or random logic signals.

1-14. The State Analyzer consists of one Model 64621A State Analysis Control Board, and from one to three State Data Acquisition Boards. The State Data Acquisition Boards may be the 40 Channel State Data Acquisition Board, the 20 Channel State Data Acquisition Board, or a combination of the two Acquisition Boards. The State Analyzer must have the necessary number of Data and Clock Probes for the Acquisition Boards used (Models 64635A and 64636A).

1-15. Up to three Acquisition Boards may be combined to form a State Analyzer with as many as 120 channels.

1-16. Logic Analyzers within one Mainframe may be connected together using the Inter Module Bus (IMB). One possible use of the IMB is to allow a State Analyzer to trigger a Timing Analyzer.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the Model 64622A. Included are initial inspection procedures, preparation for use, and instructions for repacking the instrument for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are not complete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard Office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. PREPARATION FOR USE.

2-6. There are no specific preparation for use procedures except the actual installation of the boards in the Mainframe cardcage.

2-7. INSTALLATION INSTRUCTIONS.

2-8. The 64622A Data Acquisition Board will work only when used with a 64621A State Control Board. Therefore, the installation and removal procedure is not documented here. Refer to the 64621A State Control Service Manual for installation and removal instructions. (Includes Synchronous Expansion Bus (SEB) and Inter Module Bus (IMB).)

2-9. STORAGE AND SHIPMENT.

2-10. ENVIRONMENT.

2-11. This instrument may be stored or shipped in environments within the following limits:

Temperature.....	-40 Deg C to +75 Deg C
Humidity.....	5% to 80%
Altitude.....	15000 M (50000 ft)

The instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-12. PACKING.

2-13. Tagging for Service. If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument repair number, and a description of the service required.

2-14. Original Packing. Containers and materials identical to those used in factory packing are available through Hewlett-Packard Offices. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and complete repair number.

2-15. Other Packing. The following general instructions should be used for repacking with commercially available materials:

- a. Wrap instrument in heavy plastic or paper. (If shipping to Hewlett-Packard Office or Service Center, attach a tag indicating type of service required, return address, model number, and complete repair number.
- b. Use a strong shipping container. A double wall carton made of 350 pound test material is adequate.
- c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container.
- d. Seal shipping container securely.
- e. Mark shipping container FRAGILE to ensure careful handling.
- f. In any correspondence, refer to instrument by model number and complete repair number.

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. The operation of the Model 64622A is a function of the system software. Complete operation from the keyboard of the system is beyond the scope of the Service Manual. Please refer to the Operator's Manuals for the procedure.

NOTES

SECTION IV

PERFORMANCE VERIFICATION

4-1. INTRODUCTION.

4-2. This section describes the Performance Verification (opt_test) for Model 64622A 40 Channel State Acquisition Board. This section consists of three parts; 1. Operation Verification, 2. Performance Verification, and 3. Troubleshooting.

4-3. The Operation Verification tests are all automatic and require no test equipment or dissassembly of the Mainframe. The Operation Verification provides a 90% assurance that the Model 64622A meets all specifications.

4-4. The Performance Verification tests require test equipment and dissassembly of the Mainframe. The Performance Verification tests involve manual testing and verification of specifications. Therefore, the Performance Verification Tests should be run only by a qualified service person.

4-5. The Performance Verification tests are divided into two parts; 1. automated tests and 2. manual tests. The automated tests must pass before performing the manual tests.

NOTE

Before running the following tests, insure the boards are installed as indicated in Section II of the 64621A State Analysis Service Manual. Both Operation Tests and Performance Tests must be run to insure that the Model 64622A meets all specifications after repair.

4-6. The Troubleshooting portion of this section describes the tests, shows the displays for the tests, decodes the displays, and tells how to use the tests with Signature Analysis for troubleshooting.

4-7. OPERATION VERIFICATION.

a. Press opt-test. RETURN.

b. Press SLOT # (of 40 Channel Acquisition Board) RETURN.

c. Press run all_boards. RETURN.

d. The status line near the bottom should read "STATUS: 10 MHz Verification PASSED".

e. Run the continuity tests as outlined in Section IV of the Model 64635A General Purpose Data Probe, and the Model 64636A General Purpose Clock Probe Service Manuals.

4-8. The State Control board (Control board) must pass Operation Verification before a State Acquisition board (Acquisition board) will pass.

4-9. If a failure occurred, refer to the paragraph on Troubleshooting in Section IV of the appropriate manual. This manual covers only the automatic tests for the 40 Channel Acquisition Board and signature analysis for the Data Probe interface on the 40 Channel Acquisition Board.

4-10. PERFORMANCE VERIFICATION.

4-11. First run the Automated Tests (repeat the Operation Verification), then perform the Manual Tests.

4-12. AUTOMATED TESTS.

- a. Press opt-test. RETURN.
- b. Press SLOT # of 40 Channel Acquisition Board. RETURN.
- c. Press run all_boards. RETURN.
- d. The status line near the bottom should read "STATUS: 10 MHz Verification PASSED".
- e. Run the continuity tests as outlined in Section IV of the Model 64635A General Purpose Data Probe, and the Model 64636A General Purpose Clock Probe Service Manuals.

4-13. MANUAL TESTS.

4-14. Refer to the Model 64621A State Analysis Control Board Service Manual, Section IV, Manual Tests for the procedures to test Pulse Widths, and Setup and Hold Times.

4-15. TROUBLESHOOTING.

4-16. General Comments. First, determine which of the 40 Channel Acq Board tests failed by pressing: display, SLOT # (of 40 Channel Acq Board), RETURN. Troubleshoot the first test that failed, then re-run Operation Verification. The automatic tests listed in Figure 4-1 are interdependent so that all tests preceeding a given test must pass for the given test to pass.

4-17. If the failure was a data probe and the 40 Channel Acq Board is suspected, go to the test description for the "Data Probe Interface test" which follows Test 4.

4-18. Test 5 is used in Section V, Adjustments.

4-19. Each automatic test is now described, and a signature analysis path provided. Each SA path works its way from the test output back towards the inputs. To run a particular test, press opt_test then RETURN. Press SLOT # (of the 40 Channel Acq Board) then RETURN. Finally, press run, SLOT #, test, test # (of first failing test), repeat, then RETURN. This causes the test to repeat and allows signatures to be taken. Examples of valid commands while operating the State Analysis Performance Verification are as follows:

a. run 3 test 2 RETURN . This command will cause test 2 to be performed once on the board in slot 3.

b. display 4 RETURN . This command will cause the test results of all tests on the board in slot 4 to be displayed. It will not run any test.

4-20. Various other commands are prompted by the softkeys, e.g., "repeat" makes a test cycle so that signatures may be taken; "stop" stops the test in progress; "list file name" writes the display to the designated file; "end" causes the program to leave State Analysis PV and return to option test PV.

4-21. When a bit pattern is given (e.g. data 00000100) the 1 indicates that bit 2 has failed. In all cases, a 0 indicates pass and a 1 indicates failure; the msb is to the extreme left; all patterns start with bit 0 as the lsb unless otherwise noted.

4-22. The Synchronous Expansion Bus (SEB) connects the State Control board to State Acquisition boards. The SEB is tested here for the first time. Test failure could be due to faulty seating of the SEB Cable (50 pin ribbon cable across the top of the State Cards), or to a component failure on the State Control board. Signatures for the SEB interface on the Control Board have been provided for each test as applicable. If a spare Control Board is available, it is advisable to isolate the problem to the board level before using SA. It is necessary to use an extender wire on the 5005 pod to reach the LMAP2 signal on the extender card when probing the Control board.

10 MHz State test: Board in Slot 4 Pass. Tested: 1 Failed: 0

Test	Slot 4: 40 Channel Acquisition	Tested	Failed
Automatic Tests			
1	Interaction with control board and stimulus	1	0
2	Resource Patterns	1	0
3	Sequence Patterns	1	0
4	Trace memory	1	0
Manual Tests			
5	Threshold circuit calibration	0	

Figure 4-1. Automatic Tests

4-23. Test 1: Control Board and Stimulus. Loop A

4-24. Purpose -to verify that strobe request generated by this board is received by the Control Board, and to stimulate the Data Pod Threshold D/A Converters (DACs).

4-25. How -strobe request (PBSREQ) is sent to the Control board where it resets the Slow Clock Detector.

4-26. Results -since the Strobe Generator and Slow Clock Dectector were tested during the Control Board operation verification, failure is due, most likely, to the absence of the SEB cable. "Release data bus" is a read of the mainframe data bus when nothing is addressed; failure indicates that a card in the cardcage is causing problems on the bus. The stimulus portion of this test is write-only, therefore, no results are given for it.

10 MHz State Test: Board in Slot 4 Pass Tested: 1 Failed: 0

Slot 4: 40 Channel Acquisition

Test 1: Interaction with control board and stimulus

Strobe Request Pass

Release data bus 0000000000000000

Figure 4-2. Interaction With Control Board

4-27. Stimulus -A staircase ramp is produced by the DACs during this test. See Figure 4-3. The DACs are also stimulated by Test 5.

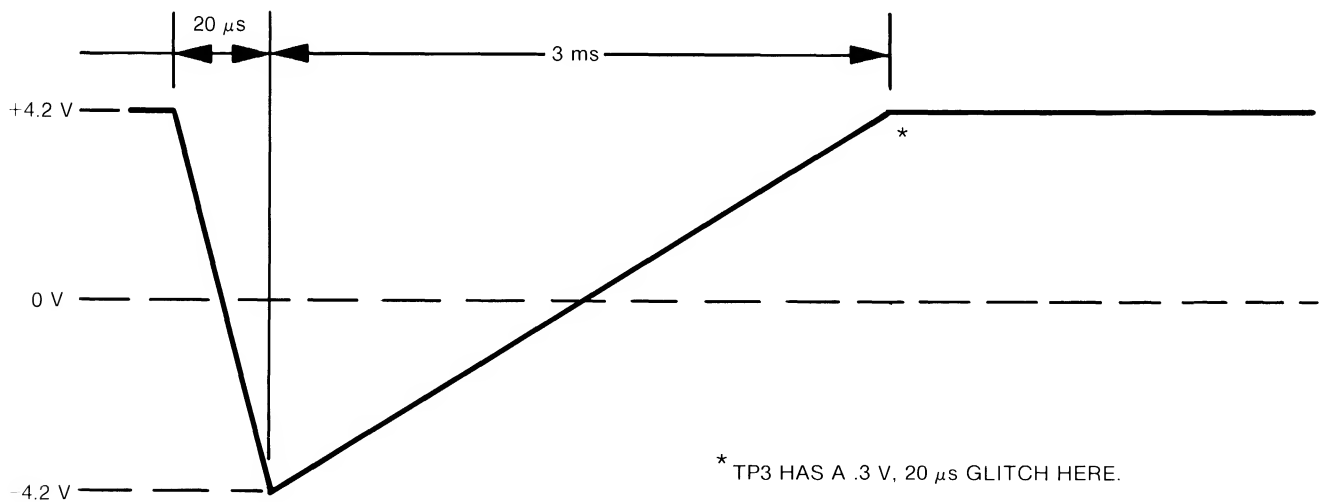


Figure 4-3. Stimulus

4-28. Loop A Signature Path for Strobe Request: U52(CTL BD), U69, U83, U114.

Loop A Singature Path for DACs: U39, U40, U68, U83, U93, U112.

4-29. Test 2: Resource Patterns. Loop B

4-30. Purpose -to verify the Mainframe Interface, the State Recognition Latch/Counters, and the Resource Pattern Recognition circuitry.

4-31. How -The Resource Pattern Trigger Memories are loaded via the Mainframe Interface and using the State Recognition Latch/Counter in the count mode. The actual Resource Patterns are bussed to the Control Board (LBRP0-7) and interpreted by the Analysis Controller. SEB signals used during this test are LBRP0-7, the state recognition strobes PBSRS and NBSRS, and strobe request PBSTBRQ.

4-32. Results -The Analysis Controller is programmed to decode the Resource Patterns (LBRP0-7) and output a trigger (NTRIG).

10 MHz State Test: Board in Slot 4 Pass. Tested: 1 Failed: 0

Slot 4: 40 Channel Acquisition
Test 2: Resource Patterns

	Bank A		Bank B
Resource Pattern:	76543210 (1 = Error)		76543210 (1 = Error)
All patterns true	00000000		00000000
All patterns false	00000000		00000000
Data bits: 0 to 3	00000000	RAM Adrs:Pass	00000000 RAM Adrs:Pass
4 to 7	00000000	Pass	00000000 Pass
8 to 11	00000000	Pass	00000000 Pass
12 to 15	00000000	Pass	00000000 Pass
16 to 19	00000000	Pass	00000000 Pass
Bank independence: Pass			

Figure 4-4. Resource Patterns

4-33. Figure 4-4 Interpretation.

	Bank A -----		Bank B -----
All patterns true	00000000	(1 = Error)	00000000 (1 = Error)
All patterns false	00000000		00000000

(Eight bit output of U22 and U7. All patterns true shows that all Acquisition boards can release the Resource Pattern circuitry and allow it to drift low. All patterns false drives the outputs high. Bank A RAMs are U62 -U66 and U76 -U80; Bank B RAMs are U70 -U74 and U84 U88.)

Data bits: 0 to 3	00000000	Pass	00000000	Pass
4 to 7	00000000	Pass	00000000	Pass
8 to 11	00000000	Pass	00000000	Pass
12 to 15	00000000	Pass	00000000	Pass
16 to 19	00000000	Pass	00000000	Pass

(Data bits, 0 to 19, represent SYND0 to SYND19 for Bank A and SYND20 to SYND39 for Bank B. They become address lines A0-A3 on the Resource Pattern Trigger Memories. The eight bit pattern output by each pair of RAMs becomes LBRP0-7. The Pass on the display refers to the RAM select lines LWR0-4.)

Bank independence: Pass (LRMSA and LRMSB test)

4-34. Loop B Signature Path: U1(CTL BD), U22, U7, Resource Pattern Trigger Memories, State Recognition Latch/Counters -U68, U83, U93, U112.

4-35. Test 3: Sequence Patterns. Loops C, D and E

4-36. Purpose -to verify Sequence Pattern Recognition Circuitry. Control Board Circuitry involved: Sequence States output by U42(CTL BD) as BSS0-3; Sequence Patterns received by U17(CTL BD) as LBSP0-3. Strobe Generator tested in Test 1 must work. Because the Control Board Sequencer contains loopback circuitry, attempt to isolate the problem before taking signatures.

4-37. How -The Sequence Pattern Trigger Memories are loaded via the Mainframe Interface and the State Recognition Latch/Counters in the count mode. Also needed for both loading and unloading the Memories (RAMs) is the Sequence State BSS0-3 provided by the Control Board Sequencer. The outputs of the RAMs are gated and sent to the Control Board as Sequence Patterns. On the Control Board, PPLS latches the Sequence State at U17, then the Sequence State is read by the Sequence Read Register. During the test, the pipeline strobe PPLS is driven by U5(CTL BD).

4-38. The outputs of the RAMs are gated so that any output stuck low will cause that bit to fail for all RAMs. Remove the RAMs one at a time and rerun the test until all bits pass for the remaining RAMs.

4-39. Three signature loops are required. The first, Loop C, checks RAM addresses and inputs from the Control Board. The second, Loop D, checks RAM outputs, and the third, Loop E, checks the inputs to the Control Board from the 40 Channel Board.

4-40. Results -all results are read by the Sequencer on the Control Board. The Acquisition board sends all Sequence Patterns as LBSP0-3 which are driven by U20.

10 MHz State Test: Board in Slot 4 Pass Tested: 1 Failed: 0

Slot 4: 40 Channel Acquisition
Test 3: Sequence Patterns

Bank A				Bank B			
Sequence RAMs:	Address	Patterns		Sequence RAMs:	Address	Patterns	
	76543210	3210			76543210	3210	
All patterns true		0000		All patterns true		0000	
All patterns false		0000		All patterns false		0000	
Data:	0 to 3	00000000	0000	Data:	0 to 3	00000000	0000
	4 to 7	00000000	0000		4 to 7	00000000	0000
	8 to 11	00000000	0000		8 to 11	00000000	0000
	12 to 15	00000000	0000		12 to 15	00000000	0000
	16 to 19	00000000	0000		16 to 19	00000000	0000

Bank Independence: Pass

Figure 4-5. Sequence Patterns

4-41. Figure 4-5 Interpretation.

	Bank A		Bank B	
	Address	Patterns	Address	Patterns
All patterns true	00000000	0000	00000000	0000
All patterns false	00000000	0000	00000000	0000

(all patterns true shows that all Acquisition boards can release the Sequence Pattern Bus and allow it to float low; the four pattern bits are the output of U20. All patterns false shows that U20 can drive LBSP0-3 high.)

Data bits: 0 to 3	00000000	0000 (U47)	00000000	0000 (U56)
4 to 7	00000000	0000 (U48)	00000000	0000 (U57)
8 to 11	00000000	0000 (U49)	00000000	0000 (U58)
12 to 15	00000000	0000 (U50)	00000000	0000 (U59)
16 to 19	00000000	0000 (U51)	00000000	0000 (U60)

(The eight bits of address and four bits of patterns represent address inputs and data outputs of the RAMs in parentheses)

Bank independence: Pass (test of LRMSA and LRMSB)

4-42. Loop C Signature Path for RAM addresses and inputs: Sequence Pattern RAMs U38, U67, U19, U18 (CTL BD), U42 (CTL BD).

4-43. Loops D and E Signature Paths for RAM outputs: U17(CTL BD), U6 (CTL BD), U20, U52-U55, Sequence Pattern RAMs.

4-44. Test 4: Trace Memory. Loops F,G,H,I,J and K**4-45. Trace Memory Read. Loop F**

4-46. Purpose -to verify functioning of the Trace Pod Data Memory. Control Board Circuitry involved -Strobe Generator which controls the write cycle timing of the Trace Memory. Signals used include PBSTBRQ, PBPLS, HBQWRT, LBMACS. Other control signals from the Control Board are P/NBDSTB, PBRSTB and LBCLR.

4-47. How -Trace Pod Data Memory (Trace Memory) consists of RAMs which receive data through a Pipeline Register and are addressed by the Memory Address Counter (MAC) and the Memory Address Selector. The RAMs are loaded by a write strobe, HBQWRT, which both enables the write function of the RAMs and increments the MAC. They are unloaded by a read strobe and a RAM selector, U91, through the latch U113. One difficulty in testing this circuit is the data source; it is the State Recognition Latch/Counters. The Counters count synchronously and load identical data into each RAM. Therefore, regardless of which RAM output is selected, the same data appears on the RAM output bus.

4-48. Results - All results are read through latch U113.

4-49. Trace Memory Write. Loops G through K

4-50. Loop G probes the addresses of the Trace Pod Data Memory (U97- U106) when the Trace Pod Memory Address Counter (U107, U109) is selected by the Trace Pod Data Memory Address Selector (U110, U108).

4-51. Loop G will find address problems that are hidden in the Loop F test. In Loop F, it is possible for the RAM outputs to be bad with all the RAM inputs good. However, Loop G catches these problems because it reads the RAMs during the write cycle.

4-52. Loops H through K. If a problem occurs in determining which RAM is degrading the bus, use the additional signature loops, H, I, J, and K, which allow for various RAMs to be removed from the board. The additional loops have the same signatures as the primary loop with the exception of RAM outputs and U113.

10 MHz State Test: Board in Slot 4 Pass Tested: 1 Failed: 0

Slot 4: 40 Channel Acquisition
Test 4: Trace memory

(1 = Error)	Address Bit	Data Channel
	76543210	9876543210987654321098765432109876543210
Data all zeroes		00
Data all ones		00
Address test	00000000	00
Address counter reset	Pass	
Store Qualification	Pass	

Figure 4-6. Trace Memory

4-53. Figure 4-6 Interpretation.

Data all zeroes	00										
Data all ones	00										
(forty bit memory:	<table border="0"> <tbody> <tr> <td>b39 - b36 = U105</td> <td>b19 - b16 = U102</td> </tr> <tr> <td>b35 - b32 = U106</td> <td>b15 - b12 = U99</td> </tr> <tr> <td>b31 - b28 = U103</td> <td>b11 - b8 = U100</td> </tr> <tr> <td>b27 - b24 = U104</td> <td>b7 - b4 = U97</td> </tr> <tr> <td>b23 - b20 = U101</td> <td>b3 - b0 = U98</td> </tr> </tbody> </table>	b39 - b36 = U105	b19 - b16 = U102	b35 - b32 = U106	b15 - b12 = U99	b31 - b28 = U103	b11 - b8 = U100	b27 - b24 = U104	b7 - b4 = U97	b23 - b20 = U101	b3 - b0 = U98
b39 - b36 = U105	b19 - b16 = U102										
b35 - b32 = U106	b15 - b12 = U99										
b31 - b28 = U103	b11 - b8 = U100										
b27 - b24 = U104	b7 - b4 = U97										
b23 - b20 = U101	b3 - b0 = U98										
Address test 00000000	00										

(eight bit address is output of U108 and U110; output selected by LBMACSEL on pin 1)

Address counter reset: Pass (U109 and U107 pin 1)

Store Qualification: Pass (HBQWRT, U5 pin 5)

4-54. Loop F Signature Path: U113, Trace Pod Data RAMs, Trace Pod Data Pipeline Register U91, U5, U111, U107-110.

4-55. Loop G Signature Path: U109, U107, U110, U108, U97 - U106.

4-56. Loop H through Loop K Signature Paths: RAMs as appropriate. Loop H has U97, U98 removed, Loop I has U97-U100 removed, etc.

4-57. Data Probe Interface Test. Loops L and M

4-58. Purpose -to test the State Recognition Latch/Counters in latch mode.

4-59. Test Conditions and Operation -to perform this test, either the General Purpose Data Probe (Loop L) or the General Purpose Preprocessor (Loop M) must be connected to the 40 Channel Acquisition board. Run the test using the command "run preprocessor test 1 repeat RETURN". Note that the inputs to the Data Probe or General Purpose Preprocessor must be open.

4-60. How -the DACs are programmed so that threshold swing at the Data Probe or GP Preprocessor causes a data pattern to be input at the State Recognition Latch/Counters. The signal LLOAD is not asserted, which allows the State Recognition circuit to parallel load data from probes (LLOAD asserted allows the Latch/Counters to count, and is used while loading the various RAMs before a run).

4-61. Results -The latched data is pipelined to the Trace Pod Data Memories and read by the Mainframe at U113. If Test 4, Trace Memory, passes, then failure of this test is due to a faulty data probe, the DACs, or the State Recognition Latch/Counter.

10 MHz State Test: Preprocessor Fail Tested: 1 Failed: 0

Preproc: GP Probes

Test 1: Clock/Data channel verification

	76543210		76543210	
Clock Edges, Positive:	00000000	Negative:	00000000	Recommendation:
Clock Qualifiers, High:	00000000	Low:	00000000	Unhook Probe
				leads
Slot	19	CHANNELS	0	
5	Pod 1:	00000000000000000000		
4	Pod 2:	00000000000000000000	Pod 3:	00000000000000000000

Figure 4-7. Data Probe Interface

4-62. Loop L and M Signature Path: U33-U37, U42-U46, U38, U41, U83, U93, U68, U39, U40.

Board # 64622-66502

Test 1: Loop A - VH = 7222

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

U 39- 3 6U29	U 69- 6 6599	U 93- 5 U793
U 39- 4 997U	U 69- 8 579P	U 93- 6 9842
U 39- 5 281H	U 69- 9 6599	U 93- 9 6263
U 39- 6 57PP	U 69-10 low	U 93-10 1UP5
U 39- 7 U195	U 69-11 6C52	
U 39- 8 9A5U	U 69-12 low	U112- 2 9CPU
U 39- 9 P9FH	U 69-13 6599	U112- 3 PU2F
U 39-11 0022		U112- 4 P87H
U 39-12 8F89	U 81- 1 5958	U112- 5 6U29
	U 81- 2 2C7A	U112- 6 83C7
U 40- 2 PU2F	U 81- 3 P414	U112- 7 997U
U 40- 3 6U29	U 81- 4 9636	U112- 8 5A3U
U 40- 4 997U	U 81- 5 H911	U112- 9 57PP
U 40- 5 281H	U 81- 6 AC33	U112-11 25FF
U 40- 6 57PP		U112-12 281H
U 40- 7 U195	U 82- 8 6599	U112-13 PC5H
U 40- 8 9A5U	U 82- 9 7222	U112-14 U195
U 40- 9 P9FH	TOTLZ OFLO	U112-15 1H0C
U 40-11 6U6U	U 82-10 7222	U112-16 9A5U
U 40-12 8F89	U 82-11 6599	U112-17 9H0P
		U112-18 P9FH
U 68- 1 2C7A	U 83- 1 17CC	U114- 1 C3UC
U 68- 2 9636	U 83- 2 6599	U114- 2 F1H9
U 68- 3 AC33	U 83- 3 0000	U114- 3 6599
U 68- 4 F3CC	TOTLZ OFLO	U114- 4 17CC
U 68- 5 65P5	U 83- 4 0022	U114- 5 0000
U 68- 6 17CC	U 83- 5 3711	TOTLZ OFLO
U 68- 7 8F89	U 83- 6 1UP5	U114- 6 7222
U 68- 9 6263	U 83-11 1UP5	TOTLZ OFLO
	U 83-12 9842	U114- 8 low
U 69- 1 17CC	U 83-13 6U6U	U114- 9 high
U 69- 2 F1H9		U114-10 7222
U 69- 3 C3UC	U 93- 1 high	U114-11 0000
U 69- 4 17CC	U 93- 3 3711	
U 69- 5 7222	U 93- 4 579P	

Board # 64622-66502

Test 1: Loop A - VH = 7222

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 8- 3 C3UC	U 24-13 C3UC ECL	U 52- 5 C3UC
	U 24-15 C3UC ECL	U 52-10 high
U 24- 9 F1H9 ECL		U 52-12 C3UC ECL
U 24-12 high ECL	U 52- 2 C3UC ECL	U 52-15 high ECL
	U 52- 4 high ECL	

Board # 64622-66502

Test 2: Loop B - VH = 55U4

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

U 4- 2 4FF3 ECL
 U 4- 3 1937 ECL
 U 4- 4 1937
 U 4- 5 1937
 U 4- 6 4FF3 ECL
 U 4- 7 1937 ECL
 U 4-10 4FF3 ECL
 U 4-11 1937 ECL
 U 4-12 1937
 U 4-13 1937
 U 4-14 4FF3 ECL
 U 4-15 1937 ECL

U 7- 3 81A8 ECL
 U 7- 4 UU21 ECL
 U 7- 5 AAH5
 U 7- 6 high
 U 7- 7 H45F
 U 7-10 5H8C
 U 7-11 8202
 U 7-12 087U ECL
 U 7-13 H7U6 ECL

U 22- 3 AU96 ECL
 U 22- 4 9476 ECL
 U 22- 5 F182
 U 22- 7 UA62
 U 22-10 AC7C
 U 22-11 7P97
 U 22-12 UP8U ECL
 U 22-13 2C63 ECL

U33 THROUGH U37
 U42 THROUGH U46
 COMMON SIGNATURES

PIN 1 CF41
 PIN 2 1937
 PIN 9 high
 PIN 11 30UP
 PIN 12 3U15
 PIN 13 F340
 PIN 14 45F1

U 41- 1 P9C5
 U 41- 2 CF41
 U 41- 3 P9C5
 U 41- 4 CF41
 U 41-12 CF41
 U 41-13 P9C5

U62 THROUGH U66
 COMMON SIGNATURES

PIN 1 30UP
 PIN 2 UA84
 PIN 4 8930
 PIN 5 F182
 PIN 6 7FA3
 PIN 7 UA62
 PIN 9 AC7C
 PIN 10 FCFC
 PIN 11 7P97
 PIN 12 C195
 PIN 13 45F1
 PIN 14 F340
 PIN 15 3U15

U 62- 3 641A

U 63- 3 7UUU

U 64- 3 37H7

U 65- 3 7AC3

U 66- 3 FH36

U 68- 1 PFU9
 U 68- 2 CHP6
 U 68- 3 81U5
 U 68- 4 8280
 U 68- 5 8280
 U 68- 6 55U4
 TOTALZ OFLO
 U 68- 7 high
 U 68- 9 A576

U 68-10 CF41
 U 68-11 FH36
 U 68-12 7AC3
 U 68-13 37H7
 U 68-14 7UUU
 U 68-15 641A

U 69- 1 55U4
 TOTALZ 14613
 U 69- 2 4FF3
 U 69- 3 1937

U70 THROUGH U74
 COMMON SIGNATURES

PIN 1 30UP
 PIN 2 20A4
 PIN 4 8930
 PIN 5 F182
 PIN 6 7FA3
 PIN 7 UA62
 PIN 9 AC7C
 PIN 10 FCFC
 PIN 11 7P97
 PIN 12 C195
 PIN 13 45F1
 PIN 14 F340
 PIN 15 3U15

U 70- 3 641A

U 71- 3 7UUU

U 72- 3 37H7

U 73- 3 7AC3

U 74- 3 FH36

U76 THROUGH U80
 COMMON SIGNATURES

PIN 1 30UP
 PIN 2 UA84

Board # 64622-66502

Test 2: Loop B - VH = 55U4

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

PIN 4 42UH	U 83- 4 UA84	U 86- 3 37H7
PIN 5 H45F	U 83- 5 AU70	
PIN 6 7F50	U 83- 6 low	U 87- 3 7AC3
PIN 7 AAH5	U 83-11 low	
PIN 9 5H8C	U 83-12 7550	U 88- 3 FH36
PIN 10 AC0C	U 83-13 20A4	
PIN 11 8202		U 93- 1 high
PIN 12 5PA0	U84 THROUGH U88	U 93- 3 AU70
PIN 13 45F1	COMMON SIGNATURES	U 93- 4 0741
PIN 14 F340		U 93- 5 933P
PIN 15 3U15	PIN 1 30UP	U 93- 6 7550
U 76- 3 641A	PIN 2 20A4	U 93- 9 A576
U 77- 3 7UUU	PIN 4 42UH	U 93-10 low
U 78- 3 37H7	PIN 5 H45F	U 93-12 42UH
U 79- 3 7AC3	PIN 6 7F50	
U 80- 3 FH36	PIN 7 AAH5	U112- 2 HFF4
U 81- 1 C90H	PIN 9 5H8C	U112- 3 5PA0
U 81- 2 PFU9	PIN 10 AC0C	U112- 4 2957
U 81- 3 P812	PIN 11 8202	U112- 5 AC0C
U 81- 4 CHP6	PIN 12 5PA0	U112- 6 9P3U
U 81- 5 H401	PIN 13 45F1	U112- 7 7F50
U 81- 6 81U5	PIN 14 F340	U112- 8 1709
U 81-12 P9C5	PIN 15 3U15	U112- 9 C195
U 81-13 CF41	U 84- 3 641A	U112-11 P461
	U 85- 3 7UUU	U112-12 42UH
		U112-13 29A4
		U112-14 FCFC
		U112-15 UPUU
		U112-16 7FA3
		U112-17 0C54
		U112-18 8930

Board # 64622-66502

Test 2: Loop B - VH = 55U4

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 1- 2 low ECL	U 1-19 55U4	TOTLZ 6931
U 1- 3 0000 ECL	TOTLZ 48256	U 1-36 high ECL
TOTLZ 25671	U 1-20 55U4	U 1-37 high ECL
U 1- 4 0000 ECL	TOTLZ 22032	U 1-38 high ECL
TOTLZ 0117	U 1-21 low ECL	U 1-39 high ECL
U 1- 7 55U4 ECL	U 1-22 H7U6 ECL	U 1-40 high ECL
TOTLZ 0256	U 1-23 UU21 ECL	
U 1- 8 low ECL	U 1-24 087U ECL	U 24- 9 4FF3 ECL
U 1- 9 POUU ECL	U 1-25 2C63 ECL	U 24-12 high ECL
U 1-12 POUU ECL	U 1-27 81A8 ECL	U 24-13 1937 ECL
U 1-15 UP8U ECL	U 1-28 9476 ECL	U 24-15 1937 ECL
U 1-16 0000 ECL	U 1-29 AU96 ECL	
TOTLZ 25671	U 1-30 high ECL	U 52- 2 1937 ECL
U 1-17 0000	U 1-33 low ECL	U 52- 4 high ECL
TOTLZ 8588	U 1-34 940C	U 52- 5 1937
U 1-18 low	U 1-35 55U4	U 52-10 high

Board # 64622-66502

Test 3: Loop C - VH = 54HA

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

U 19- 3 1FPP ECL	PIN 4 UUF6	U 67- 1 CF5H
U 19- 4 1FPP	PIN 5 80U3	U 67- 2 F266
U 19- 5 80U3	PIN 6 750F	U 67- 3 6UU6
U 19- 7 80U3 ECL	PIN 7 1FPP	U 67- 4 0375
U 19-11 750F ECL	PIN 9 HAHF	U 67- 5 94H1
U 19-12 750F	PIN 11 H062	U 67- 6 54HA
U 19-13 UA59	PIN 13 A625	TOTLZ OFLO
U 19-15 UA59 ECL	PIN 15 3UFH	U 67-11 AF88
	PIN 21 UA59	U 67-12 3HAF
U33 THROUGH U37		U 67-13 6059
U42 THROUGH U46	U 47-19 4APH	U 67-14 89F6
COMMON SIGNATURES	U 47-20 7CFP	U 67-15 7CFP
PIN 1 5FPH	U 48-19 4APH	U 81- 1 P887
PIN 2 94H1	U 48-20 89F6	U 81- 2 CF5H
PIN 9 high		U 81- 3 96CF
PIN 11 UUF6	U 49-19 4APH	U 81- 4 F266
PIN 12 CH69	U 49-20 6059	U 81- 5 3C2F
PIN 13 F7P8		U 81- 6 6UU6
PIN 14 0085	U 50-19 4APH	
	U 50-20 3HAF	U 83- 4 4APH
U 38- 1 U2UU		U 83- 5 1P37
U 38- 2 A625	U 51-19 4APH	U 83- 6 low
U 38- 3 84C8	U 51-20 AF88	U 83-11 low
U 38- 4 H062		U 83-12 94CA
U 38-10 HAHF	U 56-19 F060	U 83-13 F060
U 38-11 8P06	U 56-20 7CFP	
U 38-12 3UFH		U112- 2 HAHF
U 38-13 6C17	U 57-19 F060	U112- 4 H062
	U 57-20 89F6	U112- 6 A625
U47 THROUGH U51		U112- 9 6C17
U56 THROUGH U60	U 58-19 F060	U112-11 3UFH
COMMON SIGNATURES	U 58-20 6059	U112-14 U2UU
PIN 1 0085	U 59-19 F060	U112-16 84C8
PIN 2 F7P8	U 59-20 3HAF	U112-18 8P06
PIN 3 CH69		
	U 60-19 F060	
	U 60-20 AF88	

Board # 64622-66502

Test 3: Loop C - VH = 54HA

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 18- 2	0000	ECL	U 18-12	0000	ECL	U 42- 7	54HA	ECL
TOTLZ	2584		TOTLZ	12010		TOTLZ	8973	
U 18- 3	0000	ECL	U 18-13	0000	ECL	U 42- 8	54HA	ECL
TOTLZ	2584		TOTLZ	5818		TOTLZ	7302	
U 18- 5	low	ECL	U 18-14	0000	ECL	U 42-18	54HA	ECL
U 18- 6	high	ECL	TOTLZ	2584		TOTLZ	6323	
U 18- 7	1FPP	ECL	U 18-15	0000	ECL	U 42-19	54HA	ECL
U 18- 9	750F	ECL	TOTLZ	2584		TOTLZ	10346	
U 18-10	80U3	ECL						
U 18-11	UA59	ECL	U 42- 6	54HA	ECL			
			TOTLZ	8334				

Board # 64622-66502

Test 3: Loop D - VH = 54HA

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

U 20- 1 69P4 ECL	U 52- 4 22HA	U 55- 4 2FU7
U 20- 2 5057 ECL	U 52- 5 8772	U 55- 5 F83A
U 20- 5 5057	U 52- 6 2H67	U 55- 6 U008
U 20- 7 69P4	U 52- 9 5057	U 55- 9 2554
U 20-10 P19P	U 52-11 H780	U 55-11 69U1
U 20-11 2554	U 52-12 F95U	U 55-12 AH6H
U 20-14 2554 ECL	U 52-13 3A8C	U 55-13 H459
U 20-15 4F69 ECL	U 52-14 94A5	U 55-14 H885
	U 52-15 658F	U 55-15 94P6
U 47-10 U008		
U 47-12 PPAP	U 53- 2 2UAU	U 56-10 H885
U 47-14 48PH	U 53- 3 5HC1	U 56-12 CC5H
U 47-16 A65C	U 53- 4 1HPF	U 56-14 64U7
	U 53- 5 81C7	U 56-16 658F
U 48-10 F83A	U 53- 6 48PH	
U 48-12 74H7	U 53- 9 69P4	U 57-10 H459
U 48-14 81C7	U 53-11 F073	U 57-12 F72A
U 48-16 ACCH	U 53-12 4U68	U 57-14 78U0
	U 53-13 64U7	U 57-16 94A5
U 49-10 2FU7	U 53-14 78U0	
U 49-12 H183	U 53-15 5F53	U 58-10 69U1
U 49-14 1HPF		U 58-12 A404
U 49-16 22HA	U 54- 2 H1U3	U 58-14 5F53
	U 54- 3 129A	U 58-16 3A8C
U 50-10 4U1U	U 54- 4 H183	
U 50-12 129A	U 54- 5 PPAP	U 59-10 AH6H
U 50-14 5HC1	U 54- 6 74H7	U 59-12 P1F5
U 50-16 8772	U 54- 9 P19P	U 59-14 4U68
	U 54-11 50C9	U 59-16 F95U
U 51-10 2228	U 54-12 P1F5	
U 51-12 H1U3	U 54-13 A404	U 60-10 94P6
U 51-14 2UAU	U 54-14 F72A	U 60-12 50C9
U 51-16 2H67	U 54-15 CC5H	U 60-14 F073
		U 60-16 H780
U 52- 2 A65C	U 55- 2 2228	
U 52- 3 ACCH	U 55- 3 4U1U	

Board # 64622-66502

Test 3: Loop D - VH = 54HA

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 6-11	2554	ECL	U 17- 7	5057	ECL	U 17-11	low	ECL
U 6-14	4F69	ECL	U 17- 9	69P4	ECL			
			U 17-10	4F69	ECL			

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Test 3: Loop E - VH = F7AU

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Positive	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - U99-3 (Cntrl. Bd.)
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 6-11	F4H5	ECL	U 17- 9	0A49	ECL	U 83-11	9UF3	ECL
U 6-14	6317	ECL	U 17-10	6317	ECL	U 83-15	low	ECL
			U 17-11	low	ECL			
U 17- 2	6417	ECL	U 17-12	07H9	ECL	U 84- 3	2HP8	ECL
U 17- 3	1U21	ECL	U 17-13	35FH	ECL	U 84- 7	UF2C	ECL
U 17- 4	high	ECL	U 17-14	low	ECL	U 84-11	5HCC	ECL
U 17- 5	U644	ECL	U 17-15	9UF3	ECL	U 84-15	1CU8	ECL
U 17- 6	31PC	ECL						
U 17- 7	9HU2	ECL	U 83- 3	1U21	ECL			
			U 83- 7	6417	ECL			

Board # 64622-66502

Test 4: Loop F - VH = UUPO

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

U 5- 3 0000 ECL	U 81-10 P2A9	TOTLZ 3850
TOTLZ 0775	U 81-11 1H49	U 91-11 1H70
U 5- 4 0000		U 91-12 FHOF
TOTLZ 0775	U 82- 3 1H49	U 91-13 46H2
U 5- 5 UUPO	U 82- 4 high	U 91-14 8H85
TOTLZ 0770	U 82- 5 UUPO	U 91-15 1C2C
U 5- 6 0000 ECL	TOTLZ OFLO	
TOTLZ 0770	U 82- 6 1H49	U97 THROUGH U106
U 5-11 UUPO ECL	U 82- 8 1H49	COMMON SIGNATURES
TOTLZ 9753	U 82- 9 UUPO	PIN 1 3AFC
U 5-12 UUPO	TOTLZ OFLO	PIN 2 H6A5
TOTLZ 9753	U 82-10 UUPO	PIN 3 0C42
U 5-13 UUPO	TOTLZ 4620	PIN 4 13F6
TOTLZ 3850	U 82-11 1H49	PIN 5 3707
U 5-14 0000 ECL		PIN 6 H8C1
TOTLZ 3850	U89 AND U90	PIN 7 A907
U 5-15 UUPO ECL	U94 THROUGH U96	PIN 9 2FAU
TOTLZ 3850	COMMON SIGNATURES	PIN 10 88U1
		PIN 11 FU16
U33 THROUGH U37	PIN 1 low	PIN 12 3186
U42 THROUGH U46	PIN 2 2FAU	PIN 13 F8UA
COMMON SIGNATURES	PIN 3 2270	PIN 14 A935
	PIN 4 F3A9	PIN 15 UP56
PIN 1 1H49	PIN 5 FU16	PIN 16 109P
PIN 2 UUPO	PIN 6 F8UA	PIN 20 UUPO
TOTLZ 9753	PIN 7 F3A9	TOTLZ 0770
PIN 9 high	PIN 8 F050	PIN 21 U0H6
PIN 11 2270	PIN 9 UP56	
PIN 12 F3A9	PIN 11 0000	U 97-18 1C2C
PIN 13 F3A9	TOTLZ 0775	
PIN 14 F050	PIN 12 2FAU	U 98-18 1C2C
	PIN 13 2270	
U 81- 1 1H49	PIN 14 F3A9	U 99-18 8H85
U 81- 2 P2A9	PIN 15 FU16	
U 81- 3 UUPO	PIN 16 F8UA	U100-18 8H85
TOTLZ OFLO	PIN 17 F3A9	
U 81- 4 0000	PIN 18 F050	U101-18 46H2
TOTLZ OFLO	PIN 19 UP56	
U 81- 5 1H49		U102-18 46H2
U 81- 6 P2A9	U 91- 1 P2A9	
U 81- 8 UUPO	U 91- 2 0000	U103-18 FHOF
TOTLZ OFLO	TOTLZ OFLO	
U 81- 9 0000	U 91- 3 P2A9	U104-18 FHOF
TOTLZ OFLO	U 91- 4 UUPO	

Board # 64622-66502

Test 4: Loop F - VH = UUP0

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

U105-18 1H70	U110- 1 UUP0	U111-18 1H49
	TOTLZ 9753	U111-19 PF26
U106-18 1H70	U110- 2 5P67	
	U110- 3 56P7	U113- 1 P2A9
U107- 1 UUP0	U110- 4 A907	U113- 2 825P
TOTLZ 0006	U110- 5 FA22	U113- 3 88U1
U107- 2 UUP0	U110- 6 2751	U113- 4 3186
TOTLZ 0770	U110- 7 H8C1	U113- 5 3737
U107- 7 1H91	U110- 9 3707	U113- 6 2U94
U107-11 9217	U110-10 F8P7	U113- 7 A935
U107-12 H0F8	U110-11 F2F7	U113- 8 109P
U107-13 6211	U110-12 U0H6	U113- 9 162U
U107-14 0C70	U110-13 0U36	U113-11 UUP0
	U110-14 7C95	TOTLZ 3850
U108- 1 UUP0		U113-12 825P
TOTLZ 9753	U111- 2 56P7	U113-13 88U1
U108- 2 0C70	U111- 3 1H49	U113-14 3186
U108- 3 F52C	U111- 4 UUP0	U113-15 3737
U108- 4 3AFC	TOTLZ 0FLO	U113-16 2U94
U108- 5 6211	U111- 5 2751	U113-17 A935
U108- 6 2945	U111- 6 F8P7	U113-18 109P
U108- 7 H6A5	U111- 7 UUP0	U113-19 162U
U108- 9 0C42	TOTLZ 0FLO	
U108-10 U4A2	U111- 8 UUP0	U114- 5 0000
U108-11 H0F8	TOTLZ 0FLO	TOTLZ 0FLO
U108-12 13F6	U111- 9 0U36	U114- 6 UUP0
U108-13 PF26	U111-11 0000	TOTLZ 0FLO
U108-14 9217	TOTLZ 3850	U114-10 UUP0
	U111-12 F52C	TOTLZ 4620
U109- 1 UUP0	U111-13 UUP0	U114-11 0000
TOTLZ 0006	TOTLZ 0FLO	TOTLZ 4620
U109- 2 UUP0	U111-14 UUP0	U114-12 UUP0
TOTLZ 0770	TOTLZ 0FLO	TOTLZ 3850
U109-11 7C95	U111-15 2945	U114-13 0000
U109-12 F2F7	U111-16 U4A2	TOTLZ 3850
U109-13 FA22	U111-17 UUP0	
U109-14 5P67	TOTLZ 0FLO	
U109-15 1H91		

Board # 64622-66502

Test 4: Loop F - VH = UUP0

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Control Board Signatures (ICs on Control Board)

U 5- 3 0000 ECL	TOTLZ 0006	U 43-10 0000 ECL
TOTLZ 0775	U 8-13 0000	TOTLZ 9753
U 5- 6 0000 ECL	TOTLZ 0006	U 43-11 0000 ECL
TOTLZ 9753		TOTLZ 9753
U 5- 7 7UUP ECL	U 16- 9 UUP0 ECL	U 43-12 0000 ECL
U 5-10 0000 ECL	TOTLZ 9753	TOTLZ 9753
TOTLZ 9753	U 16-12 0000 ECL	U 43-13 0000 ECL
U 5-11 7CUA ECL	TOTLZ 9753	TOTLZ 9753
U 5-12 UUP0 ECL	U 16-13 0000 ECL	U 43-14 UUP0 ECL
TOTLZ 9753	TOTLZ 9753	TOTLZ 13603
U 5-13 UUP0 ECL		
TOTLZ 9753	U 19- 2 0000 ECL	U 85- 1 0000 ECL
U 5-14 0000 ECL	TOTLZ 3850	TOTLZ 3850
TOTLZ 0770	U 19- 3 UUP0 ECL	U 85- 7 0000
U 5-15 UUP0 ECL	TOTLZ 3850	TOTLZ 3850
TOTLZ 9753	U 19- 4 UUP0 ECL	
	TOTLZ 3850	U102- 7 UUP0
U 8- 8 0000	U 19- 5 UUP0 ECL	TOTLZ 0006
TOTLZ 0006	TOTLZ 13603	
U 8- 9 UUP0	U 19- 6 0000 ECL	U125- 1 0000
TOTLZ 0006	TOTLZ 3850	TOTLZ 3850
U 8-10 UUP0	U 19- 7 0000 ECL	U125- 2 UUP0
TOTLZ 0006	TOTLZ 3850	TOTLZ 17526
U 8-11 UUP0		U125- 3 UUP0
TOTLZ 0006	U 43- 9 0000 ECL	TOTLZ 0FLO
U 8-12 0000	TOTLZ 3850	

Board # 64622-66502

Test 4: Loop G - VH = 5U91

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - U101-20
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

U97 THROUGH U106 COMMON SIGNATURES	U107- 2 5U91 TOTLZ 0770	U109- 1 5U91 TOTLZ 0006
PIN 1 6297	U107- 7 470A	U109- 2 5U91
PIN 2 7P7A	U107-10 470A	TOTLZ 0770
PIN 3 0F39	U107-11 29P7	U109-11 3C64
PIN 4 7676	U107-12 53A8	U109-12 8H2C
PIN 5 H2CA	U107-13 21PC	U109-13 C985
PIN 6 P614	U107-14 3H06	U109-14 FA8U
PIN 7 951P	U108- 1 0000	U109-15 470A
PIN 8 low	TOTLZ 9753	U110- 1 0000
PIN 9 2H5U	U108- 2 3H06	TOTLZ 9753
PIN 11 43C1	U108- 3 1658	U110- 2 FA8U
PIN 13 3545	U108- 4 6297	U110- 3 1658
PIN 15 HC58	U108- 5 21PC	U110- 4 951P
PIN 18 5U91	U108- 6 1658	U110- 5 C985
TOTLZ 0770	U108- 9 0F39	U110- 6 1658
PIN 20 5U91	U108-10 1658	U110- 9 H2CA
TOTLZ 0770	U108-11 53A8	U110-10 1658
PIN 21 64U5	U108-12 7676	U110-11 8H2C
U107- 1 5U91	U108-13 1658	U110-12 64U5
TOTLZ 0006	U108-14 29P7	U110-13 1658
		U110-14 3C64

Board # 64622-66502

Test 4: Loop H - VH = UUPO

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Remove RAMs U97 through U98.

U99 THROUGH U106
COMMON SIGNATURES

PIN 10 0470
PIN 12 H8FC
PIN 14 H48A
PIN 16 4847

Note: Signatures for RAM inputs are the same as LOOP E signatures.

Board # 64622-66502

Test 4: Loop I - VH = UUPO

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Remove RAMs U97 through U100.

U101 THROUGH U106
COMMON SIGNATURES

PIN 10 4230
PIN 12 2F6H
PIN 14 6A55
PIN 16 P42C

Note: Signatures for RAM inputs are the same as LOOP E signatures.

Board # 64622-66502

Test 4: Loop J - VH = UUPO

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Remove RAMs U97 through U102.

U103 THROUGH U106
COMMON SIGNATURES

PIN 10 P110
PIN 12 563P
PIN 14 353A
PIN 16 C21H

Note: Signatures for RAM inputs are the same as LOOP E signatures.

Board # 64622-66502

Test 4: Loop K - VH = UUPO

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Remove RAMs U97 through U104.

U105 AND U106
COMMON SIGNATURES

PIN 10 4P69
PIN 12 95UP
PIN 14 9A8H
PIN 16 1916

Note: Signatures for RAM inputs are the same as LOOP E signatures.

Board # 64622-66502

Gen. Pur. Probes Test: Loop L - VH = P733

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Connect Model 64635A, General Purpose Probes, to 64622A J3 and J4 cables. 5005A set up and the signatures are on the 64622A running the test "preprocessor test 1".

U 4- 2 0000 ECL	U 38- 5 6A70	U42 THROUGH U46
TOTLZ 0051	U 38- 6 8H43	COMMON SIGNATURES
U 4- 3 P733 ECL	U 38- 8 8H43	PIN 1 high
TOTLZ 0050	U 38- 9 6A70	PIN 2 P733
U 4- 4 P733		TOTLZ 0050
TOTLZ 0050	U 39- 2 U56A	PIN 3 1P01
U 4- 5 P733	U 39- 3 UFP8	PIN 4 1P01
TOTLZ 0050	U 39- 4 UFP8	PIN 5 1P01
U 4- 6 0000 ECL	U 39- 5 UFP8	PIN 6 1P01
TOTLZ 0051	U 39- 6 7H82	PIN 9 8H43
U 4- 7 P733 ECL	U 39- 7 7H82	PIN 11 001U
TOTLZ 0050	U 39- 8 7H82	PIN 12 001U
U 4-10 0000 ECL	U 39- 9 7H82	PIN 13 001U
TOTLZ 0051	U 39-11 0PUF	PIN 14 001U
U 4-11 P733 ECL	U 39-12 PPC1	
TOTLZ 0050		U 68- 1 0982
U 4-12 P733	U 40- 2 U56A	U 68- 2 9CPF
TOTLZ 0050	U 40- 3 UFP8	U 68- 3 9CPF
U 4-13 P733	U 40- 4 UFP8	U 68- 4 7FHU
TOTLZ 0050	U 40- 5 UFP8	U 68- 5 7FHU
U 4-14 0000 ECL	U 40- 6 7H82	U 68- 6 9CPF
TOTLZ 0051	U 40- 7 7H82	U 68- 7 PPC1
U 4-15 P733 ECL	U 40- 8 7H82	U 68- 9 755H
TOTLZ 0050	U 40- 9 7H82	
	U 40-11 83CU	U 83- 4 0PUF
	U 40-12 PPC1	U 83- 5 P9FU
		U 83- 6 6A70
	U 41- 1 low	U 83-11 6A70
	U 41- 2 high	U 83-12 648F
	U 41- 3 low	U 83-13 83CU
	U 41- 4 high	
	U 41- 5 6A70	U 93- 1 high
	U 41- 6 8H43	U 93- 3 P9FU
	U 41- 8 8H43	U 93- 4 62U0
	U 41- 9 6A70	U 93- 5 71U4
	U 41-10 8H43	U 93- 6 648F
	U 41-11 6A70	U 93- 9 755H
	U 41-12 high	U 93-10 6A70
	U 41-13 low	U 93-12 UFP8
		U 93-15 6A70

U33 THROUGH U37
COMMON SIGNATURES

PIN 1 high
PIN 2 P733
TOTLZ 0050
PIN 3 197U
PIN 4 197U
PIN 5 197U
PIN 6 197U
PIN 9 8H43
PIN 11 001U
PIN 12 001U
PIN 13 001U
PIN 14 001U

Board # 64622-66502

Gen. Pur. Probes Test: Loop L - VH = P733

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Connect Model 64635A, General Purpose Probes, to 64622A J3 and J4 cables. 5005A set up and the signatures are on the 64622A running the test "preprocessor test 1".

U112- 8	1CHC	TP3	1P01
U112-12	UFP8		
TP2	197U		

Board # 64622-66502

Preprocessor Test: Loop M - VH = 5159

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Plug 64622A J3 cable into Preprocessor POD 1 and 64622A J4 cable into Preprocessor POD 2. Remove all user inputs to the Preprocessor.

U 4- 2	0000	ECL	U 12- 5	08A9		U 18- 7	08A9	ECL
TOTLZ	0048		U 12- 6	59U0	ECL	U 18-10	59U0	ECL
U 4- 3	5159	ECL	U 12- 7	08A9	ECL	U 18-11	08A9	ECL
TOTLZ	0048		U 12-10	59U0	ECL	U 18-12	08A9	
U 4- 4	5159		U 12-11	08A9	ECL	U 18-13	08A9	
TOTLZ	0048		U 12-12	08A9		U 18-14	59U0	ECL
U 4- 5	5159		U 12-13	08A9		U 18-15	08A9	ECL
TOTLZ	0048		U 12-14	59U0	ECL			
U 4- 6	0000	ECL	U 12-15	08A9	ECL	U 23- 2	67F3	ECL
TOTLZ	0048					U 23- 3	369A	ECL
U 4- 7	5159	ECL	U 14- 2	59U0	ECL	U 23- 4	369A	
TOTLZ	0048		U 14- 3	08A9	ECL	U 23- 5	369A	
U 4-10	0000	ECL	U 14- 4	08A9		U 23- 6	67F3	ECL
TOTLZ	0048		U 14- 5	08A9		U 23- 7	369A	ECL
U 4-11	5159	ECL	U 14- 6	59U0	ECL	U 23-10	67F3	ECL
TOTLZ	0048		U 14- 7	08A9	ECL	U 23-11	369A	ECL
U 4-12	5159		U 14-10	59U0	ECL	U 23-12	369A	
TOTLZ	0048		U 14-11	08A9	ECL	U 23-13	369A	
U 4-13	5159		U 14-12	08A9		U 23-14	67F3	ECL
TOTLZ	0048		U 14-13	08A9		U 23-15	369A	ECL
U 4-14	0000	ECL	U 14-14	59U0	ECL			
TOTLZ	0048		U 14-15	08A9	ECL	U 25- 2	9PU1	ECL
U 4-15	5159	ECL				U 25- 3	FUA8	ECL
TOTLZ	0048		U 16- 2	59U0	ECL	U 25- 4	FUA8	
			U 16- 3	08A9	ECL	U 25- 5	FUA8	
U 10- 2	59U0	ECL	U 16- 4	08A9		U 25- 6	9PU1	ECL
U 10- 3	08A9	ECL	U 16- 5	08A9		U 25- 7	FUA8	ECL
U 10- 4	08A9		U 16- 6	59U0	ECL	U 25-10	9PU1	ECL
U 10- 5	08A9		U 16- 7	08A9	ECL	U 25-11	FUA8	ECL
U 10- 6	59U0	ECL	U 16-10	59U0	ECL	U 25-12	FUA8	
U 10- 7	08A9	ECL	U 16-11	08A9	ECL	U 25-13	FUA8	
U 10-10	59U0	ECL	U 16-12	08A9		U 25-14	9PU1	ECL
U 10-11	08A9	ECL	U 16-13	08A9		U 25-15	FUA8	ECL
U 10-12	08A9		U 16-14	59U0	ECL			
U 10-13	08A9		U 16-15	08A9	ECL	U 27- 2	9PU1	ECL
U 10-14	59U0	ECL				U 27- 3	FUA8	ECL
U 10-15	08A9	ECL	U 18- 2	59U0	ECL	U 27- 4	FUA8	
			U 18- 3	08A9	ECL	U 27- 5	FUA8	
U 12- 2	59U0	ECL	U 18- 4	08A9		U 27- 6	9PU1	ECL
U 12- 3	08A9	ECL	U 18- 5	08A9		U 27- 7	FUA8	ECL
U 12- 4	08A9		U 18- 6	59U0	ECL	U 27-10	9PU1	ECL

Board # 64622-66502

Preprocessor Test: Loop M - VH = 5159

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Plug 64622A J3 cable into Preprocessor POD 1 and 64622A J4 cable into Preprocessor POD 2. Remove all user inputs to the Preprocessor.

U 27-11	FUA8	ECL	PIN 6	08A9	U 41- 9	3U64
U 27-12	FUA8		PIN 9	6P3H	U 41-10	6P3H
U 27-13	FUA8		PIN 11	P672	U 41-11	3U64
U 27-14	9PU1	ECL	PIN 12	P672	U 41-12	high
U 27-15	FUA8	ECL	PIN 13	P672	U 41-13	low
			PIN 14	P672		
U 29- 2	9PU1	ECL			U 42- 1	high
U 29- 3	FUA8	ECL	U 38- 5	3U64	U 42- 2	5159
U 29- 4	FUA8		U 38- 6	6P3H	TOTLZ	0048
U 29- 5	FUA8		U 38- 8	6P3H	U 42- 3	369A
U 29- 6	9PU1	ECL	U 38- 9	3U64	U 42- 4	369A
U 29- 7	FUA8	ECL			U 42- 5	369A
U 29-10	9PU1	ECL	U 39- 2	C7A6	U 42- 6	369A
U 29-11	FUA8	ECL	U 39- 3	UF70	U 42- 9	6P3H
U 29-12	FUA8		U 39- 4	UF70	U 42-11	P672
U 29-13	FUA8		U 39- 5	UF70	U 42-12	P672
U 29-14	9PU1	ECL	U 39- 6	0812	U 42-13	P672
U 29-15	FUA8	ECL	U 39- 7	0812	U 42-14	P672
			U 39- 8	0812	U 42-15	P672
U 31- 2	9PU1	ECL	U 39- 9	0812		
U 31- 3	FUA8	ECL	U 39-11	729C	U43 THROUGH U46	
U 31- 4	FUA8		U 39-12	1A8U	COMMON SIGNATURES	
U 31- 5	FUA8					
U 31- 6	9PU1	ECL	U 40- 2	C7A6	PIN 1	high
U 31- 7	FUA8	ECL	U 40- 3	UF70	PIN 2	5159
U 31-10	9PU1	ECL	U 40- 4	UF70	TOTLZ	0048
U 31-11	FUA8	ECL	U 40- 5	UF70	PIN 3	FUA8
U 31-12	FUA8		U 40- 6	0812	PIN 4	FUA8
U 31-13	FUA8		U 40- 7	0812	PIN 5	FUA8
U 31-14	9PU1	ECL	U 40- 8	0812	PIN 6	FUA8
U 31-15	FUA8	ECL	U 40- 9	0812	PIN 9	6P3H
			U 40-11	1FA6	PIN 11	9954
			U 40-12	1A8U	PIN 12	9954
U33 THROUGH U37					PIN 13	9954
COMMON SIGNATURES					PIN 14	9954
			U 41- 1	low	PIN 15	9954
PIN 1	high		U 41- 2	high		
PIN 2	5159		U 41- 3	low		
TOTLZ	0048		U 41- 4	high	U 68- 1	4CH6
PIN 3	08A9		U 41- 5	3U64	U 68- 2	2819
PIN 4	08A9		U 41- 6	6P3H	U 68- 3	2819
PIN 5	08A9		U 41- 8	6P3H	U 68- 4	7940

Board # 64622-66502

Preprocessor Test: Loop M - VH = 5159

MODE:	EDGES:	THRESHOLDS:	CONNECTIONS:
Normal	Clock - Negative	Data - High **	ST/SP/Start - LMAP2
-----	Start - Positive	Data - Low **	Qual/Stop - LMAP2
-----	Stop - Negative	Clock - TTL	Clock - TP4
-----		ST-SP-QL - TTL	Ground - GND

** = levels are TTL except where noted.

Plug 64622A J3 cable into Preprocessor POD 1 and 64622A J4 cable into Preprocessor POD 2. Remove all user inputs to the Preprocessor.

U 68- 5 7940	U 83-11 3U64	U 93-10 3U64
U 68- 6 2819	U 83-12 4HUU	U 93-12 UF70
U 68- 7 1A8U	U 83-13 1FA6	U 93-15 3U64
U 68- 9 3296		
U 68-10 high	U 93- 1 high	U112- 8 AH29
	U 93- 3 23F2	U112-12 UF70
U 83- 4 729C	U 93- 4 210U	
U 83- 5 23F2	U 93- 5 C6A2	TP2 U6P5
U 83- 6 3U64	U 93- 6 4HUU	TP3 FUA8
	U 93- 9 3296	

NOTES

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section describes adjustments and checks required to return the instrument to peak operating capability after repairs have been made.

5-3. SAFETY REQUIREMENTS.

5-4. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summary at the front of this manual or with specific warnings given throughout the manual could result in serious injury or death or damage to equipment. Service adjustments should be performed only by qualified service personnel.

5-5. EQUIPMENT REQUIRED.

5-6. 4 1/2 Digit Voltmeter with +/-1 mV accuracy. (Hewlett-Packard Model 3466A or equivalent.)

5-7. PROCEDURE.

5-8. This procedure assumes that all other modules of this system are working properly, and all are calibrated and meet or exceed their respective specifications.

NOTE

Installation and removal of PC Boards must be done with the A.C. Power for the Mainframe turned off.

5-9. Threshold Adjustments.

- a. Acquisition Board adjustments may be made with or without the Control Board installed in the Mainframe.
- b. Place the 40 Channel Acquisition Board on an extender board. The IMB and SEB Bus Cables do not need to be connected.
- c. If they are not already disconnected, disconnect the Data Probe Cables from J3 and J4.
- d. Connect the ground lead of the DMM to TP6 GND. See figure 5-1.
- e. Connect the positive lead of the DMM to Testpoint 2 (Pod A).
- f. Select `opt_test` , press RETURN . The display will indicate the option modules present and the card slot number they are located in.
- g. Press "slot number", RETURN . "Slot number" is a number from 0 to 9 equal to the location of the 40 Channel ACQ Board.

- h. Press run , "slot number" , test , 5 , RETURN . The CRT should now display "Test 5: Threshold Circuit Calibration".
- i. Each time the RETURN key is pressed, the D/A Converter will be set to a new value. Press RETURN until "Reference = -4.267 V Negative Limit" is displayed.
- j. Adjust -FS, R2, to -4.267 V +/- 1 mV. See figure 5-1.
- k. Move the positive lead of the DMM to TP3 (Pod B). Note the voltage at TP3.
- l. If the voltage at TP3 is more positive than -4.267, go to step m. If the voltage at TP3 is more negative than -4.267 go to step p.
- m. Find the difference between the voltage at TP3 and -4.267. Divide the difference by 2.
- n. Using -FS, R2, readjust R2 for -4.267 plus the value found in step m +/-1 mV (difference divided by 2).
- o. For a quick check move the positive lead of the DMM to TP2. The value at TP2 should be -4.267 minus the value in step m +/-1 mV. If TP2 is not the correct value, go back to step j and repeat the procedure. If it is the correct value go to step s.

NOTE

The average value of TP2 and TP3 should be -4.267 V.

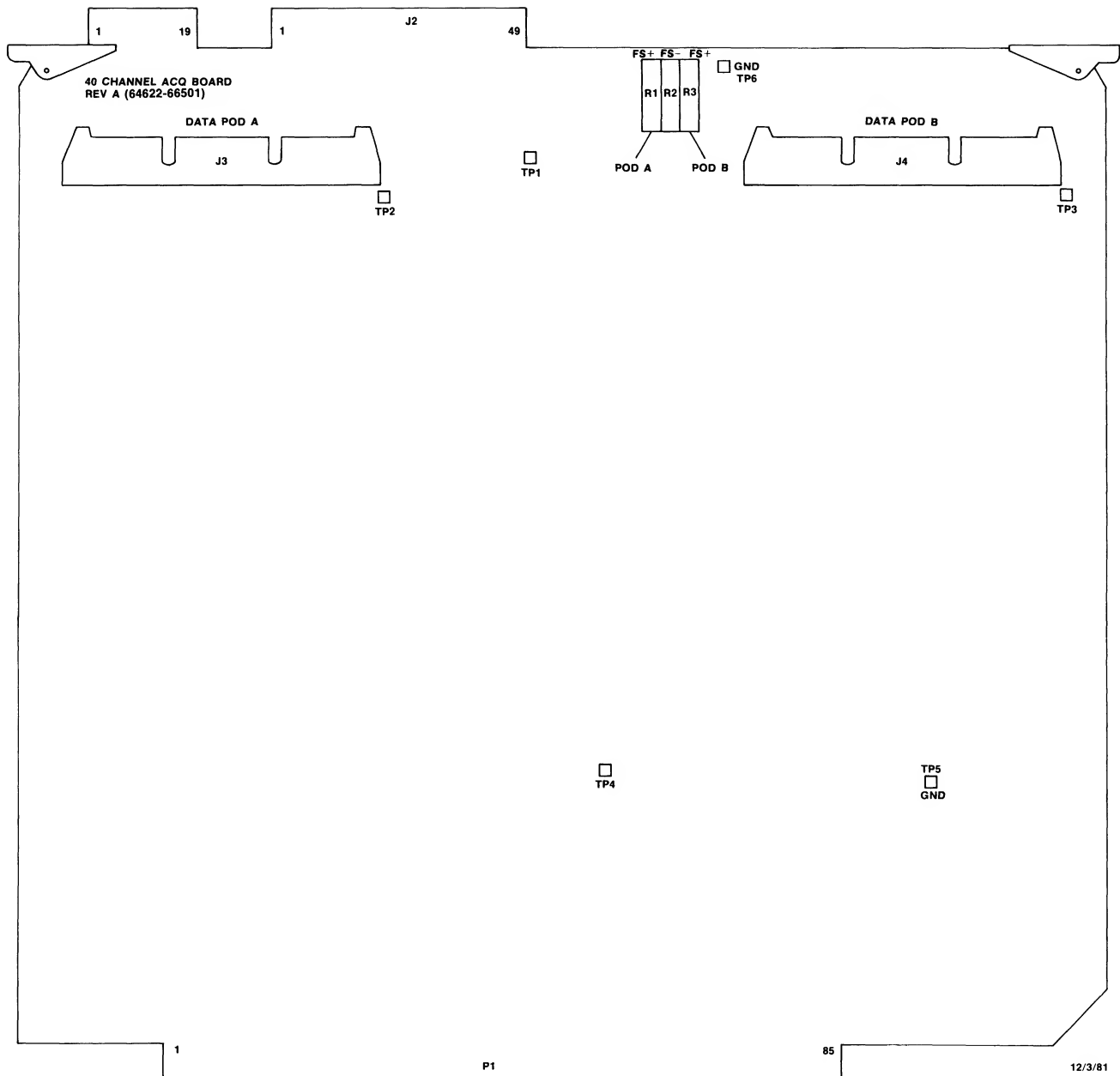
- p. Find the difference between the voltage at TP3 and -4.267. Divide the difference by 2.
- q. Using -FS, R2, readjust R2 for -4.267 minus the value found in step p +/-1 mV (difference divided by 2).
- r. For a quick check move the positive lead of the DMM to TP2. The value at TP2 should be -4.267 plus the value in step p +/-1 mV. If TP2 is not the correct value, go back to step j and repeat the procedure. If it is the correct value go to step s.

NOTE

The average value of TP2 and TP3 should be -4.267 V.

- s. Continue pressing RETURN until "Reference = +433 mV ECL (-1.3 V)" is displayed. (You should still be on TP2.)
- t. Adjust +FS, R1 (Pod A), to +433 mV. See figure 5-1.
- u. Each time RETURN is pressed, the D/A Converter will be set to a different value. Press RETURN six times and verify that the value measured on the DMM is within +/-33 mV of the value displayed for all six DAC levels. (If the voltages are not correct, there is most likely a problem in the DAC and must be corrected using the Performance Verification.)

- v. Connect the positive lead of the DMM to TP3 (Pod B).
- w. Continue pressing RETURN until "Reference = +433 mV ECL (-1.3 V)" is displayed.
- x. Adjust +FS, R3 (Pod B), to +433 mV. See figure 5-1.
- y. Each time RETURN is pressed, the D/A Converter will be set to a different value. Press RETURN six times and verify that the value measured on the DMM is within ± 33 mV of the value displayed for all six DAC levels. (If the voltages are not correct, there is most likely a problem in the DAC and must be corrected using the Performance Verification.)
- z. Press end , RETURN , end , to exit the 40 Channel Acquisition Performance Verification.

*Figure 5-1. Adjustment Locations*

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

- a. Chassis-mounted parts in alphanumerical order by reference designation.
- b. Electrical assemblies and their components in alphanumerical order by reference designation.
- c. Miscellaneous parts.

The information given for each part consists of the following:

- a. The Hewlett-Packard part number and the check digit.
- b. The total quantity (Qty) in the instrument.
- c. The description of the part.
- d. A five-digit code that indicates the manufacturer.
- e. The manufacturers' part number.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of

the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-10. SPARE PARTS KIT.

6-11. A spare parts kit is not available at this time.

6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

- a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.
- b. No Maximum or minimum on any mail order (there is a minimum order amount, for parts ordered through a local HP office when the orders require billing and invoicing).
- c. Prepaid transportation (there is a small handling charge for each order).
- d. No invoices -to provide these advantages, a check or money order must accompany each order.

6-14. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS							
A	= assembly	F	= fuse	MP	= mechanical part	U	= integrated circuit
B	= motor	FL	= filter	P	= plug	V	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	IC	= integrated circuit	Q	= transistor	VR	= voltage regulator
C	= capacitor	J	= jack	R	= resistor	W	= cable
CP	= coupler	K	= relay	RT	= thermistor	X	= socket
CR	= diode	L	= inductor	S	= switch	Y	= crystal
DL	= delay line	LS	= loud speaker	T	= transformer	Z	= tuned cavity network
DS	= device signaling (lamp)	M	= meter	TB	= terminal board		
E	= misc electronic part	MK	= microphone	TP	= test point		
ABBREVIATIONS							
A	= amperes	H	= henries	N/O	= normally open	RMO	= rack mount only
AFC	= automatic frequency control	HDW	= hardware	NOM	= nominal	RMS	= root-mean square
AMPL	= amplifier	HEX	= hexagonal	NPO	= negative positive zero (zero temperature coefficient)	RWV	= reverse working voltage
BFO	= beat frequency oscillator	HG	= mercury	NPN	= negative-positive-negative	S-B	= slow-blow
BE CU	= beryllium copper	HR	= hour(s)	NRFR	= not recommended for field replacement	SCR	= screw
BH	= binder head	HZ	= hertz	NSR	= not separately replaceable	SE	= selenium
BP	= bandpass	IF	= intermediate freq			SECT	= section(s)
BRS	= brass	IMPG	= impregnated			SEMICON	= semiconductor
BWO	= backward wave oscillator	INCD	= incandescent			SI	= silicon
CCW	= counter-clockwise	INCL	= include(s)	OBD	= order by description	SIL	= silver
CER	= ceramic	INS	= insulation(ed)	OH	= oval head	SL	= slide
CMO	= cabinet mount only	INT	= internal	OX	= oxide	SPG	= spring
COEF	= coefficient	K	= kilo=1000			SPL	= special
COM	= common			P	= peak	SST	= stainless steel
COMP	= composition	LH	= left hand	PC	= printed circuit	SR	= split ring
COMPL	= complete	LIN	= linear taper	PF	= picofarads= 10 ⁻¹² farads	STL	= steel
CONN	= connector	LK WASH	= lock washer	PH BRZ	= phosphor bronze	TA	= tantalum
CP	= cadmium plate	LOG	= logarithmic taper	PHL	= phillips	TD	= time delay
CRT	= cathode-ray tube	LPF	= low pass filter	PIV	= peak inverse voltage	TGL	= toggle
CW	= clockwise			PNP	= positive-negative-positive	THD	= thread
DEPC	= deposited carbon	M	= milli=10 ⁻³	P/O	= part of	TI	= titanium
DR	= drive	MEG	= meg=10 ⁶	POLY	= polystyrene	TOL	= tolerance
ELECT	= electrolytic	MET FLM	= metal film	PORC	= porcelain	TRIM	= trimmer
ENCAP	= encapsulated	MET OX	= metallic oxide	POS	= position(s)	TWT	= traveling wave tube
EXT	= external	MFR	= manufacturer	POT	= potentiometer		
F	= farads	MHZ	= mega hertz	PP	= peak-to-peak	U	= micro=10 ⁻⁶
FH	= flat head	MINAT	= miniature	PT	= point	VAR	= variable
FIL H	= fillister head	MOM	= momentary	PWV	= peak working voltage	VDCW	= dc working volts
FXD	= fixed	MOS	= metal oxide substrate			W/	= with
		MTG	= mounting	RECT	= rectifier	W	= watts
		MY	= "mylar"	RF	= radio frequency	WIV	= working inverse voltage
G	= giga (10 ⁹)	N	= nano (10 ⁻⁹)	RH	= round head or right hand	WW	= wirewound
GE	= germanium	N/C	= normally closed			W/O	= without
GL	= glass	NE	= neon				
GRD	= grounded	NI PL	= nickel plate				

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64622A	4		40-CHANNEL STATE DATA ACQUISITION BOARD	28480	64622A
A1	64622-66501	6	1	40-CHANNEL STATE DATA ACQUISITION BOARD	28480	64622-66501
A1C1	0160-2055	9	49	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C3	0160-0576	5	2	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C4	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C11	0160-0178	3	2	CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-0178
A1C12	0160-0178	3		CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-0178
A1C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C19	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C38	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C39	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C42	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C44	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C45	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C46	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C47	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C48	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C49	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C51	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C52	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C53	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C54	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C55	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C56	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C57-58	0160-3456	6	2	CAPACITOR-FXD .001UF +80-20% 1KVDC CER	28480	0160-3456
A1J3	1251-6651	3	2	CONNECTOR 50-PIN M POST TYPE	28480	1251-6651
A1J4	1251-6651	3		CONNECTOR 50-PIN M POST TYPE	28480	1251-6651
A1MP1	64622-85001	1	1	EXTRACTOR-P.C. BOARD	28480	64622-85001
A1MP2	64622-85002	2	1	EXTRACTOR-P.C. BOARD	28480	64622-85002
A1MP3	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
A1MP4	1480-0116	8		PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
A1R1	2100-3123	0	3	RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R2	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R3	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A1R4	0698-3152	8	2	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A1R4	0698-3154	0	2	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A1R5	0757-0283	6	6	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R6	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R7	0698-3152	8		RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A1R8	0757-0442	9	3	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R9	0757-0437	2	2	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R10	0757-0437	2	2	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A1R11	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A1R12	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R13	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R15	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R16	0757-0283	6	7	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R17	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R18	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R19	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R20	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R21	0757-0280	3	3	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R22	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R23	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R24	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R25	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R26	0757-0442	9	3	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R27	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R28	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R29	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1TP1	0360-0535	0	6	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1U1	1826-0271	0	2	IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A1U2	1826-0271	0		IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A1U3	1820-2359	7		IC MISC ECL 14-INP	07263	F10014PC
A1U4	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U5	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U6	1810-0275	1	2	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A1U7	1820-1173	1		IC XLTR ECL TTL-T0-ECL QUAD 2-INP	04713	MC10124L
A1U8	1826-0544	0		V REF 8-DIP-C	04713	MC1403U
A1U9	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U10	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U11	1810-0298	8	5	NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U12	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U13	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U14	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U15	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U16	1820-1052	5	5	IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U17	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U18	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U19	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U20	1820-1173	1		IC XLTR ECL TTL-T0-ECL QUAD 2-INP	04713	MC10124L
A1U21	1810-0275	1	1	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A1U22	1820-1173	1		IC XLTR ECL TTL-T0-ECL QUAD 2-INP	04713	MC10124L
A1U23	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U24	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U25	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U26	1810-0298	8	5	NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U27	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U28	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U29	1820-1052	5		IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U30	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U31	1820-1052	5	10	IC XLTR ECL ECL-T0-TTL QUAD 2-INP	04713	MC10125L
A1U32	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
A1U33	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U34	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U35	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U36	1820-1475	6	4	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U37	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U38	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U39	1826-0856	7		IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A1U40	1826-0856	7		IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A1U41	1820-1199	1	6	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U42	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U43	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U44	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U45	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U46	1820-1475	6	10	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U47	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U48	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U49	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U50	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U51	1816-1476	8	4	IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U52	1820-1130	0		IC GATE TTL S NAND 13-INP	01295	SN74S133N
A1U53	1820-1130	0		IC GATE TTL S NAND 13-INP	01295	SN74S133N
A1U54	1820-1130	0		IC GATE TTL S NAND 13-INP	01295	SN74S133N
A1U55	1820-1130	0		IC GATE TTL S NAND 13-INP	01295	SN74S133N
A1U56	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U57	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U58	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U59	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U60	1816-1476	8		IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U61	1810-0270	6	2	NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
A1U62	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U63	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U64	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U65	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U66	1816-0787	2	2	IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U67	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U68	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U69	1820-0269	4		IC GATE TTL NAND QUAD 2-INP	01295	SN7403N
A1U70	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U71	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U72	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U73	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U74	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U75	1810-0270	6		NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
A1U76	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U77	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U78	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U79	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U80	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U81	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U82	1820-1203	8		IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A1U83	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U84	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U85	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U86	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U87	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U88	1816-0787	2		IC TTL S 64-BIT STAT RAM 35-NS 0-C	01295	SN74S289N
A1U89	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U90	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U91	1820-2550	0	1	IC DCDR TTL LS 3-TO-8-LINE	01295	SN74LS137N
A1U93	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A1U94	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U95	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U96	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U97	1816-1308	5	10	IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U98	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U99	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U100	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U101	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U102	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U103	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U104	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U105	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U106	1816-1308	5		IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U107	1820-1430	3	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U108	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A1U109	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U110	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A1U111	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A1U112	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A1U113	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U114	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1XU1	1200-0796	8	2	SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1XU2	1200-0796	8		SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1XU10	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU14	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU16	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU18	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU23	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU25	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU27	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU29	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU31	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU62	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU63	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU64	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU65	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1XU66	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU70	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU71	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU72	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU73	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU74	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU76	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU77	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU78	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU79	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU80	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU84	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU85	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU86	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU87	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU88	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU97	1200-0612	7	10	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU98	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU99	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU100	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU101	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU102	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU103	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU104	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU105	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU106	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
MP1	2200-0147	4	2	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP2	2200-0151	0	2	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP3	64620-67601	7	1	HOOD-CONNECTOR ASSEMBLY (TOP)	28480	64620-67601
MP4	64620-67602	8	1	HOOD-CONNECTOR ASSEMBLY (BOTTOM)	28480	64620-67602
MP5	7121-2163	5	1	LABEL-DATA PROBE	28480	7121-2163
W2	64620-61601	5	1	CABLE-DATA ASSEMBLY	28480	64620-61601

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address	Zip Code
50167	FUJITSU LTD	TOKYO JP	
54013	HITACHI	TOKYO JP	
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW CA	94042
11236	CTS OF BERNE INC	BERNE IN	46711
19701	HEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
20932	EMCON DIV ITW	SAN DIEGO CA	92129
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
25403	AMPEREX ELEK CORP SEMICON & MC DIV	SLATERSVILLE RI	02876
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA	95051
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE NJ	
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE CA	94086
52763	STETTNER-TRUSH INC	CAZENOVIA NY	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE SC	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA PA	19108

SECTION VII

MANUAL BACKDATING

7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for a specific repair number prefix.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the repair number prefix shown on the manual title page. If the repair prefix is not the same as the one on the title page, find your repair number prefix in Table 7-1 and make the changes to the manual that are listed for that repair number prefix. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1,2 and 3 are required for your repair number, do change 3 first, then change 2, and finally change 1.

7-5. If the repair number of your instrument is not listed either on the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA corrections.

Table 7-1. Manual Changes

PREFIX	MAKE CHANGES
2144A	1

CHANGE 1

Section V

Pages 40ACQ 5-1 through 40ACQ 5-4.

Replace all of the pages in Section V with pages 5-1 thru 5-4 from this Backdating Section.

Section VI

Page 40ACQ 6-4, Table 6-2. Replaceable Parts List.

Change the part number for A1 from 64622-66502 to 64622-66501, and the check digit from 7 to 6.

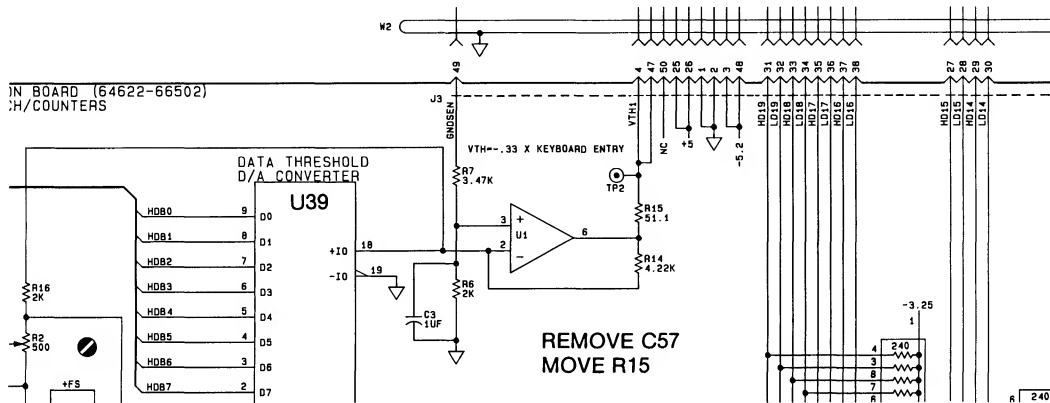
Delete A1C57 and 58, 0160-3456, 6, -, CAPACITOR-FXD .001UF +80-20% 1000VDC CER, 28480, 1060-3456.

Section VIII

Delete C57 and C58 from the eight component locators facing the schematics.

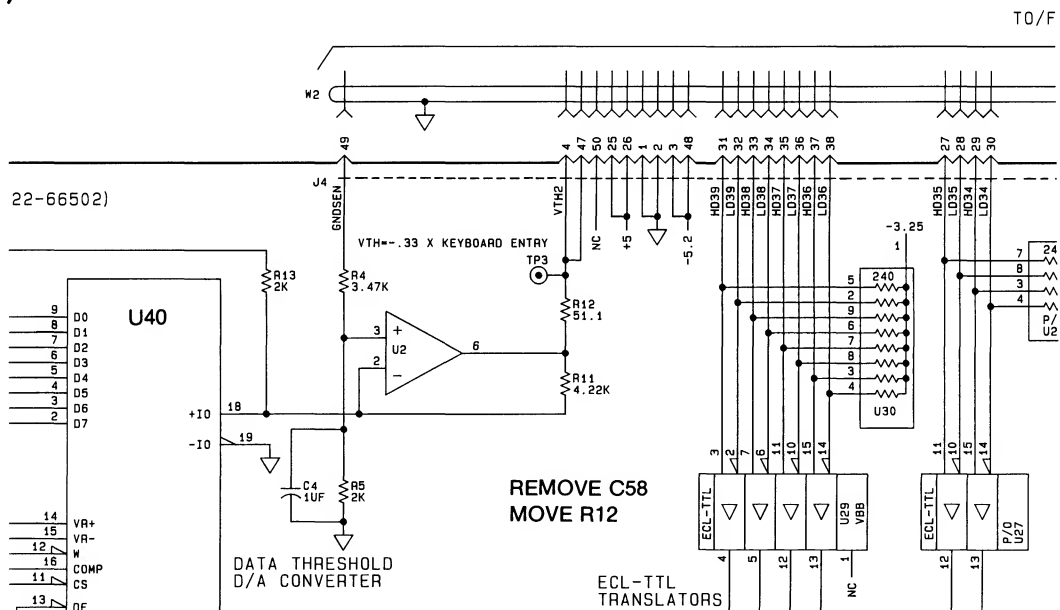
Page 40ACQ 8-7, Service Sheet 1.

Change the schematic in the area of U1 as shown below: (remove C57, and move R15)



Page 40ACQ 8-9, Service Sheet 2.

Change the schematic in the area of U2 as shown below: (remove C58 and move R12)



SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section describes adjustments and checks required to return the instrument to peak operating capability after repairs have been made.

5-3. SAFETY REQUIREMENTS.

5-4. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summary at the front of this manual or with specific warnings given throughout the manual could result in serious injury or death or damage to equipment. Service adjustments should be performed only by qualified service personnel.

5-5. EQUIPMENT REQUIRED.

5-6. 4 1/2 Digit Voltmeter with +/-1 mV accuracy. (Hewlett-Packard Model 3466A or equivalent).

5-7. PROCEDURE.

5-8. This procedure assumes that all other modules of this system are working properly, and all are calibrated and meet or exceed their respective specifications.

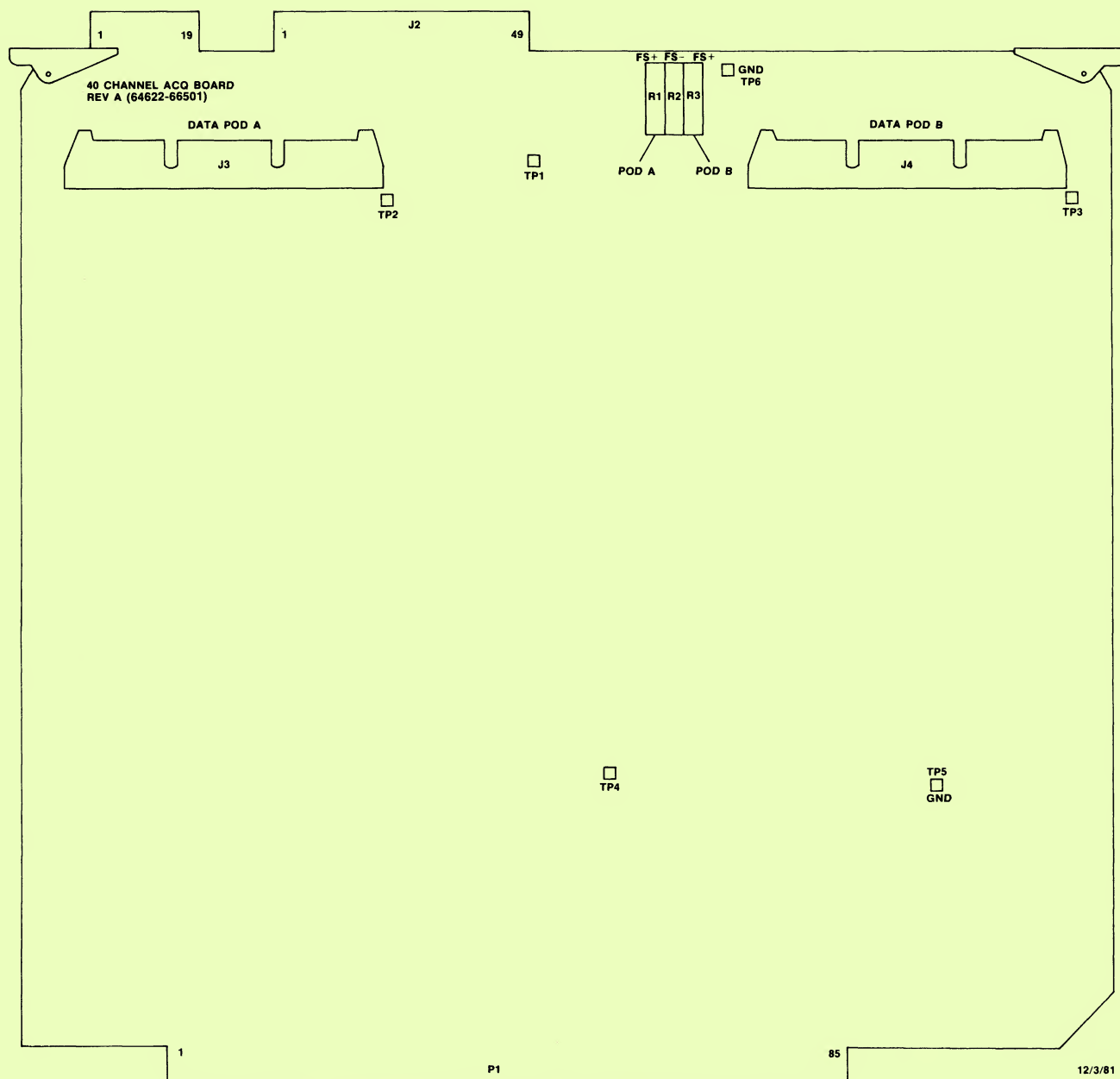
NOTE

Installation and removal of PC Boards must be done with the A.C. Power for the Mainframe turned off.

5-9. Threshold Adjustments.

- a. Acquisition Board adjustments may be made with or without the Control Board installed in the Mainframe.
- b. Place the 40 Channel Acquisition Board on an extender board. The IMB and SEB Bus Cables do not need to be connected.
- c. If they are not already disconnected, disconnect the Data Probe Cables from J3 and J4.
- d. Connect the ground lead of the DMM to TP6 GND. See figure 5-1.
- e. Using a jumper wire, connect TP2 and TP3 together.
- f. Connect the positive lead of the DMM to Testpoint 2 (Pod A).
- g. Select `opt_test` , press RETURN . The display will indicate the option modules present and the card slot number they are located in.

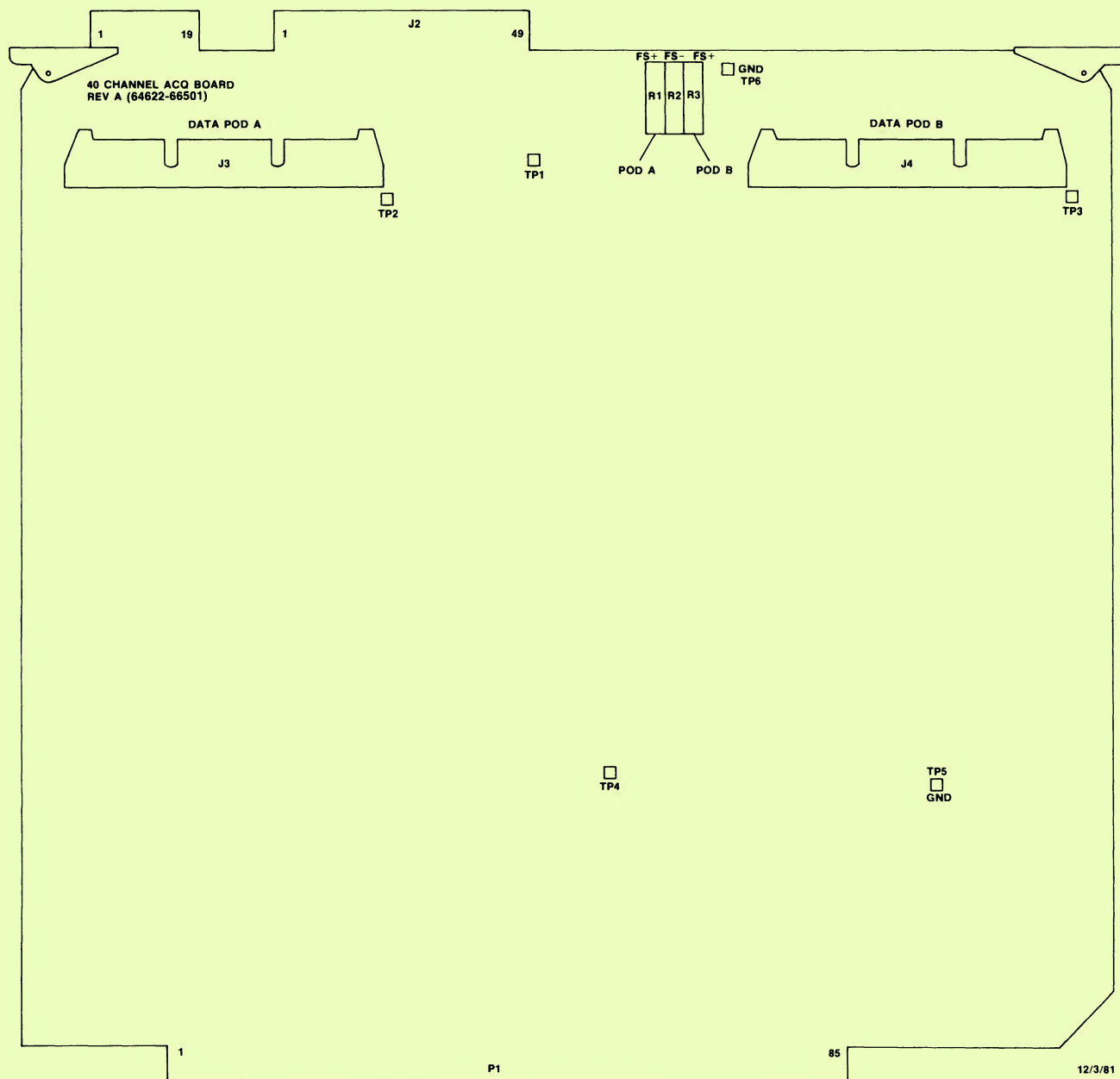
- h. Press "slot number", RETURN . "Slot number" is a number from 0 to 9 equal to the location of the 40 Channel ACQ Board.
- i. Press run , "slot number" , test , 5 , RETURN . The CRT should now display "Test 5: Threshold Circuit Calibration".
- j. Each time the RETURN key is pressed, the D/A Converter will be set to a new value. Press RETURN until "Reference = -4.267 V Negative Limit" is displayed.
- k. Adjust -FS, R2, to -4.267 V +/- 1 mV. See figure 5-1.
- l. Remove the jumper from TP2 and TP3. The positive lead of the DMM remains on TP2 (Pod A).
- m. Continue pressing RETURN until "Reference = +433 mV ECL (-1.3 V)" is displayed.
- n. Adjust +FS, R1 (Pod A), to +433 mV. See figure 5-1.
- o. Each time RETURN is pressed, the D/A Converter will be set to a different value. Press RETURN six times and verify that the value measured on the DMM is within +/-33 mV of the value displayed for all six DAC levels. (If the voltages are not correct, there is most likely a problem in the DAC and must be corrected using the Performance Verification.)
- p. Connect the positive lead of the DMM to TP3 (Pod B).
- q. Continue pressing RETURN until "Reference = +433 mV ECL (-1.3 V)" is displayed.
- r. Adjust +FS, R3 (Pod B), to +433 mV. See figure 5-1.
- s. Each time RETURN is pressed, the D/A Converter will be set to a different value. Press RETURN six times and verify that the value measured on the DMM is within +/-33 mV of the value displayed for all six DAC levels. (If the voltages are not correct, there is most likely a problem in the DAC and must be corrected using the Performance Verification.)
- t. Press end , RETURN , end to exit the 40 Channel Acquisition Performance Verification.

*Figure 5-1. Adjustment Locations*

Model 64622A

Adjustments

NOTES

*Figure 5-1. Adjustment Locations*

NOTES

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains information for troubleshooting and repairing the Model 64622A 40 Channel State Acquisition Board.

8-3. The block diagram, schematic, component location figure, and other service information are provided on fold-out service sheets to help you in servicing the Model 64622A.

8-4. Normally, Theory of Operation is provided in this Section. However, the Model 64622A 40 Channel State Acquisition Board cannot function without a Model 64621A State Analysis Control Board, and for the purpose of the Theory of Operation, the two models are considered as one unit. Therefore, only limited Theory of Operation is provided in this manual. The Model 64621A State Analysis Control Board Service Manual, Section VIII, Service, provides more Theory of Operation at the State Analyzer Subsystem level.

8-5. Because the 40 Channel State Acquisition Board is very software dependent, it becomes very difficult to discuss the Theory of Operation at the bit level. Therefore, the following discussion is at the concept level of various functions.

8-6. 40 CHANNEL BLOCK DIAGRAM.

8-7. The Model 64622A 40 Channel State Acquisition Board consists of the following five basic functional groups:

- * State Recognition Latch/Counter and D/A Converters
- * Resource Pattern Recognition
- * Sequence Pattern Recognition
- * Trace Pod Data Memory
- * Mainframe Interface

8-8. 40 CHANNEL BLOCK DIAGRAM THEORY.

8-9. STATE RECOGNITION LATCH/COUNTER.

- * When in the latch mode, the State Recognition Latch, U33-37, U42-46, captures incoming data from the Data Probe.
- * The information is latched using the clock strobe coming from the Control Board.
- * When in the count (load) mode, the outputs of U33-37, U42-46, are used for stimulating the State Analyzer during Performance Verification and for loading the Resource and Sequence Pattern Recognition RAMs.
- * The D/A Converters set the threshold for the Data Probes, and are controlled by the keyboard.

8-10. RESOURCE PATTERN RECOGNITION.

* The Resource Pattern Recognition circuitry is a group of Random Access Memories (RAMs) and 8 translators used to recognize patterns of data from the State Recognition Latches.

* The information to be analyzed is used to address the memories. When the address (information) is equal to the location at which ones were stored, those ones will appear at the outputs of the memories, thus indicating that the event has been recognized.

* The translators send the Resource Patterns to the Analysis Control Board.

8-11. SEQUENCE PATTERN RECOGNITION.

* The Sequence Pattern Recognition circuitry is a group of Random Access Memories and several gates used to recognize sequences of data from the State Recognition Latches.

* The sequence state and the information to be analyzed is used to address the memories. When the address (information) is equal to the location at which ones were stored, those ones will appear at the outputs of the memories, thus indicating that the sequence pattern has been found.

* This information is sent to the Sequencer on the Control Board.

8-12. TRACE POD DATA MEMORY.

* The Trace Pod Data Memory consists of RAMs, latches (Pipeline Register) and data selectors for chip selection, and address counters.

* The Pipeline Register, U89, U90, U94-U96, holds information until the memories are ready to accept the information to be stored.

* The memories, U97-U105, store 256 words of the information being analyzed, to be formatted by the Mainframe CPU and displayed on the CRT at a later time.

* The data selectors provide the addresses for the memories. In the write mode, the addresses come from the Address Counters, U107, U109. In the read mode, the addresses come from the Mainframe CPU.

8-13. MAINFRAME INTERFACE.

* The Mainframe Interface consists of various latches and buffers for interfacing the State Analyzer's circuits to the Mainframe.

* Through the use of read and write decoders, the Mainframe can select various groups of circuitry on the Control Board and write to (program) or read from (verify, interrogate) them over the Mainframes Data Bus.

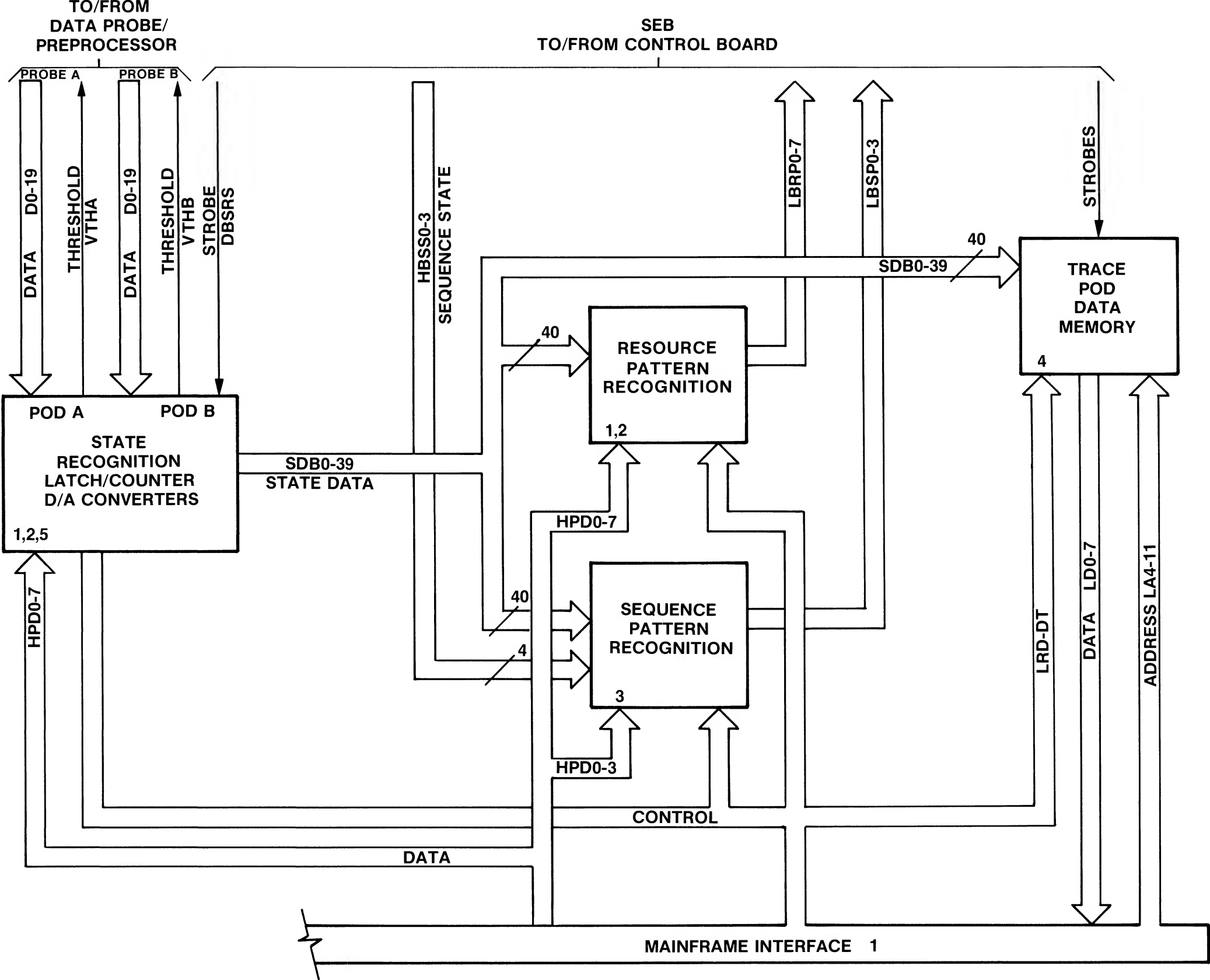


Figure 8-1.
40 Channel ACQ Block Diagram
40ACQ 8-3

8-14. MNEMONICS.

8-15. The signals in this product have been assigned mnemonics that indicate the true state, and the function of the signal line. In general the first character indicates the true state, H for high, L for low. If the signal is used with an edge sensitive device, P for positive, and N for negative is used to indicate the edge that the signal becomes true on. No indication of the voltage levels is given, i.e., TTL, ECL, MOS. This information is given on the schematic using the newer type of Logic Symbology.

Table 8-1. Mnemonics

Mnemonic	Description
-FS	Minus Full Scale -- a voltage reference used to control the negative limit of the threshold reference output by the Digital to Analog Converters for Data Pods A and B.
BSS0-3	Bus Sequence State 0-3 -- a feed back path within the Control Board Sequencer that enables it to change from one state to the next. A state may require that an event occur only once, or it may require the event to occur many times before changing to the next state. BSS0-3 develops SSB0-3.
GNDSSEN	Ground Sense -- the return path from the Data Probe for the Data Threshold Digital to Analog Converters.
HAB0-2	High Address Buffered 0-2 -- same as the CPU Address Bus (LA4-11) except inverted. HAB0-2 is used to develop select lines for the Trace Pod Data Memories (LSEL0-4).
HBQWRT	High Bus Qualified Write -- when high, HBQWRT synchronizes data storage in the Trace Pod Data Memories in the Acquisition Boards with the Trace Counter/Status Memories in the Control Board. When low, HBQWRT increments the Trace Pod Data Memory Address Counters on the Data Acquisition Boards. HBQWRT is enabled by HWQ, and is derived from HWRT on the Control Board.
HCLRCNT	High Clear Counter -- a signal generated by the CPU. When high, HCLRCNT resets the State Recognition Latch/Counters for Pod A and Pod B.
HD0-39	High Data 0-39 -- differential data signals (LD0-39) generated by the equipment being monitored. HD0-39 may come from either the Data Probes or the Preprocessor.
HDB0-7	High Data Buffered 0-7 -- same as the CPU Data Bus (LD0-7) except inverted. HDB0-7 is the path the CPU uses when it wants to input data to various circuits on the Data Acquisition Board.
HLOAD	High Load -- a signal generated by the CPU. When low, the State Recognition Latch/Counters are in the count mode.
HMA0-7	High Memory Address 0-7 -- developed by the Trace Pod Data Memory Address Counters or the CPU (LA4-11). Used to address the Trace Pod A and B Data Memories.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
HRP0-7	High Resource Pattern 0-7 -- outputs of the Resource Pattern Memories. When high, indicates that combinations of Trigger, Storage, and Count information have been detected. HRP0-7 becomes LBRP0-7 and is sent to the Control Board.
HSEQ0-39	High Sequence 0-39 -- outputs of the Pod Sequence Pattern Memories. When decoded, HSEQ0-39 produce LBSP0-3.
LA0-13	Low Address 0-13 -- a 16 bit address bus used by the CPU to address various devices in the system. The Address Bus is transmit only from the CPU. Only bits 0-13 are used in this model.
LBCLR	Low Bus Clear -- LBCLR comes from the Control Board. When low, LBCLR clears the Trace Pod Data Memory Address Counter.
LBMACS	Low Bus Memory Address Counter Select -- developed in the Control Board Strobe Generator. In the 40 Channel Data Acquisition Board, LBMACS allows the Memory Address Counters to address the Trace Pod Data Memories when low. When high, the CPU can address the Memories over the CPU Address Bus.
LBRP0-7	Low Bus Resource Pattern 0-7 -- eight signals going to the Control Board. When low, indicates to the Analysis Controller that combinations of Trigger, Storage, and Count information have been detected.
LBSP0-3	Low Bus Sequence Pattern 0-3 -- four signals going to the Control Board. When low, they indicate to the Sequencer that the Data Acquisition Boards have found the Sequence State(s) requested by the user.
LCLRCNT	Low Clear Count -- developed from HCLRCNT. When low, LCLRCNT resets the State Recognition Latch/Counters for Pod A and Pod B.
LD0-12	Low Data 0-12 --a 16 bit bidirectional bus used to transfer data to and from the CPU. When LSTB is low, the data on the bus is valid. Only bits 0-9 and bit 12 are used in this model.
LD0-39	Low Data 0-39 -- differential data signals (HD0-39) generated by the equipment being monitored. LD0-39 may come from either the Data Probes or the Preprocessor.
LDB0-3	Low Data Buffered 0-3 -- same as the CPU Data Bus except buffered. LDB0-3 is a path the CPU uses when it wants to input data to the Pod Sequence Pattern Memories.
LID	Low Identification -- a signal originating in the Mainframe. When low, the CPU is requesting that the Board Identification be sent from the State Analyzer Data Acquisition Board to the CPU over the Data Bus on data bits 9 and 12.
LLOAD	Low Load -- a signal generated by the CPU. When low, the State Recognition Latch/Counters are in the count mode.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LMAP2	Low Map 2 -- a signal developed by the CPU. LMAP2 is used as the Start/Stop Pulse in Signature Analysis and appears only on the extender card.
LPOP	Low Power On Preset -- when low (during Mainframe power-up or during A.C. power line disturbances), LPOP resets various latches, counters, and registers to a known state. When LPOP returns to a high state, the Mainframe begins executing software.
LQWS	Low Qualified Write Strobe -- same as HBQWRT except inverted. When low, LQWS allows data to be written to the Trace Pod Data Memories. When going from a low state to a high state, LQWS increments the Trace Pod Data Memory Address Counters.
LRMSA	Low Resource Memory Select A -- developed by the CPU in the Write Decoders. When low, LRMSA enables Pod A Resource Pattern Memories and the Data Threshold D/A Converter.
LRMSB	Low Resource Memory Select B -- developed by the CPU in the Write Decoders. When low, LRMSB enables Pod B Resource Pattern Memories and the Data Threshold D/A Converter.
LSEL	Low Select -- a signal originating in the Mainframe. When low, LSEL allows the State Analyzer Identification Code to be returned over the CPU's Data Bus. This allows the CPU to identify if there is a State Analyzer Data Acquisition Board installed in the Mainframe, and if so which slot of the Card Cage it is installed in. LSEL is also used to enable the State Analyzer Data Acquisition Board.
LSTB	Low Strobe -- when low and the CPU is in the write mode (LWRT low), LSTB indicates the Data Bus has valid information on it. When low and in the read mode, LSTB indicates that the CPU is not driving the Data Bus, and the device addressed may now drive it.
LTMS0-4	Low Trace Memory Select 0-4 -- developed by the CPU in the RAM Selector. LTMS0-4 enables the outputs of the Trace Pod Data Memories.
LWR0-4	Low Write Resource 0-4 -- developed by the CPU in the Write Decoders. When low, LWR0-4 allows the CPU to write information into the Resource Pattern Memories (HDB0-7).
LWRT	Low Write -- one of the control lines from the Mainframe. When low, the CPU is writing to the addressed device, i.e., the State Analyzer Data Acquisition Board.
LWS0-4	Low Write Sequence 0-4 -- developed by the CPU in the Write Decoders. When low, LWS0-4 allows the CPU to write information into the Sequence Pattern Memories (LDB0-7).

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
LWTHR	Low Write Threshold -- when LWTHR goes from a high state to a low state, information from the CPU is latched into the Digital to Analog Converter. The output current is proportional to the binary value latched. ((Full Scale Current X Binary Value Latched)/256 = Output Current.
NBDSTB	Negative Bus Data Strobe -- a differential signal (PBDSTB), developed in the Control Board Strobe Generator. Used to latch the outputs of the Trace Pod Data Memories into the Trace Pod Data Latch on the Data Acquisition Boards.
NBSRS	Negative Bus State Recognition Strobe -- a differential strobe (PBSRS) developed in the Control Board Strobe Generator, and sent to the Data Acquisition Boards. At the beginning of a data acquisition cycle, NBSRS goes from a high state to a low state. NBSRS is used to latch user information into the State Recognition Latch/Counters.
PBDSTB	Positive Bus Data Strobe -- a differential signal (NBDSTB), developed in the Control Board Strobe Generator. Used to latch the outputs of the Trace Pod Data Memories into the Trace Pod Data Latch on the Data Acquisition Boards.
PBPLS	Positive Bus Pipeline Strobe - used in the 40 Channel Data Acquisition Board for latching user information into Trace Pod Data Pipeline Registers at the correct time in the Analyzer's timing cycle.
PBRSTB	Positive Bus Read Strobe -- developed by the Control Board Strobe Generator. When PBRSTB goes from a low to a high state, the read address for the Trace Pod Data Memories is latched into the Memory Address Latch. When going from a high state to a low state, PBRSTB latches the Trace Pod Data Memory select line (LTMS0-4) into the RAM Selector.
PBSRS	Positive Bus State Recognition Strobe -- a differential strobe (NBSRS) developed in the Control Board Strobe Generator, and sent to the Data Acquisition Boards. At the beginning of a data acquisition cycle, PBSRS goes from a low state to a high state. PBSRS is used to latch user information into the State Recognition Latch/Counters.
PBSTERQ	Positive Bus Strobe Request -- a signal going to the Control Board during Performance Verification only. When going from a low to a high state, PBSTERQ begins a strobe generator cycle. PBSTERQ is wire ORed with PPVSTB and HMCLK on the Control Board.
PPLSTB	Positive Pipeline Strobe -- same as PBPLS except buffered. PPLSTB latches target system information into the Trace Pod Data Pipeline Registers at the correct time in the Analyzer's timing cycle.
SD0-7	State Data 0-7 -- an eight bit path from the Trace Pod Data Memories to the Trace Pod Data Latch. The CPU uses this path along with the CPU Data Bus to read information out of the Trace Pod Data Memories.

Table 8-1. Mnemonics (Cont'd)

Mnemonic	Description
SSB0-3	Sequence State Buffered 0-3 -- same as BSS0-3 except buffered. BSS0-3 are developed by the Control Board Sequencer and enables it to change from one state to the next. A state may require that an event occur only once, or it may require the event to occur many times before changing to the next state.
SYND0-39	Synchronous Data 0-39 -- a data path from the State Recognition Latch/Counters to the Resource Pattern Memories, the Sequence Pattern Memories, and the Trace Pod Data Pipeline Registers.
SYNPD0-39	Synchronous Pipelined Data 0-39 -- a data path from the Trace Pod Data Pipeline Register to the Trace Pod Data Memories.
VREF	Voltage, Reference -- a reference voltage of 2.5 V used by the Data Threshold Digital to Analog Converters for Data Pods A and B.
VTH1	Voltage, Thershold 1 -- a user programmable voltage sent to the Data Probe as a reference voltage for the Comparators.
VTH2	Voltage, Thershold 2 -- a user programmable voltage sent to the Data Probe as a reference voltage for the Comparators.

Table 8-2. Schematic Diagram Notes


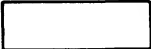










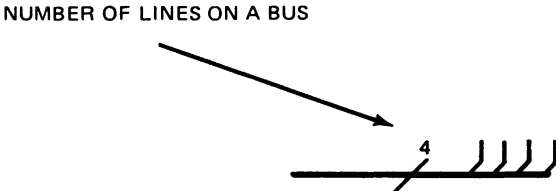
	ETCHED CIRCUIT BOARD	(925)	WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE
	FRONT PANEL MARKING		[(925) IS WHT-RED-GRN]
	REAR-PANEL MARKING		0 - BLACK 5 - GREEN 1 - BROWN 6 - BLUE 2 - RED 7 - VIOLET 3 - ORANGE 8 - GRAY 4 - YELLOW 9 - WHITE
	MANUAL CONTROL		
	SCREWDRIVER ADJUSTMENT		
 TP1	ELECTRICAL TEST POINT TP (WITH NUMBER)		* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.
	NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.		UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS CAPACITANCE IN PICOFARADS INDUCTANCE IN MICROHENRIES
	LETTERED TEST POINT NO MEASUREMENT AID PROVIDED	μP = MICROPROCESSOR P/O = PART OF NC = NO CONNECTION CW = CLOCKWISE END OF VARIABLE RESISTOR	
	COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.		
 3	NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION. LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.		
	CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.		
	INDICATES SINGLE SIGNAL LINE		
	NUMBER OF LINES ON A BUS		

Table 8-3. Logic Symbology

Table 8-3. Logic Symbology (Cont'd)

Table 8-3. Logic Symbology (Cont'd)

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

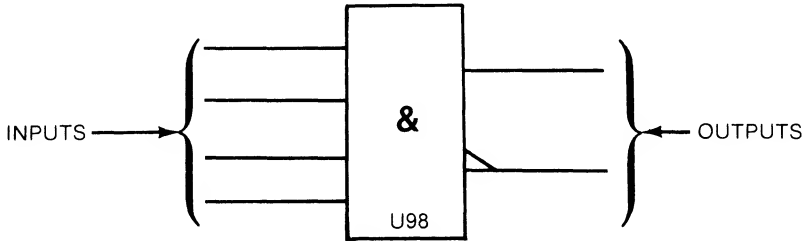
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

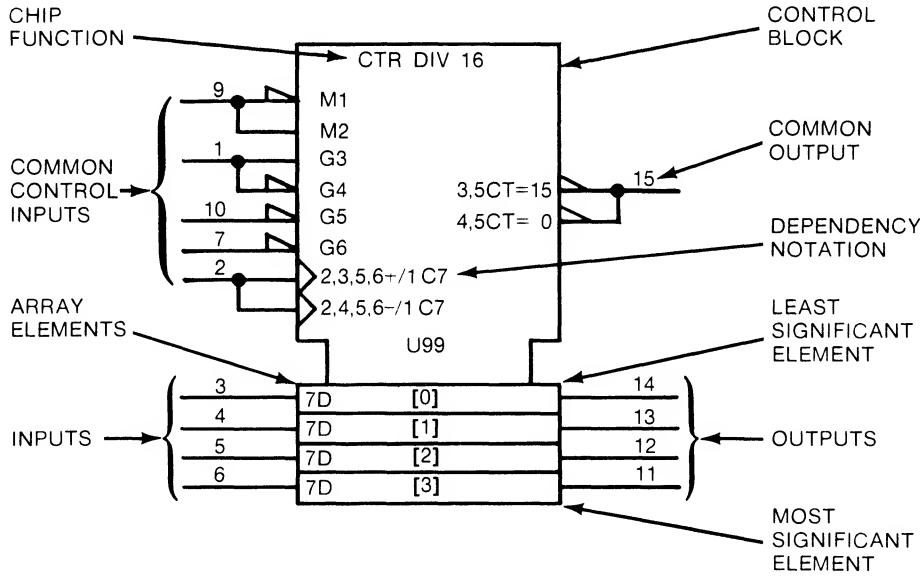
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in []).

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INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

- AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.
- Interconnection (Z) indicates connections inside the symbol.
- Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.
- Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.
- Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).
- Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.
- Address (A) identifies the address inputs.
- Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (complements state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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OTHER SYMBOLS

Analog Signal	Inversion	Shift Right (or down)
AND	Negation	Solidus (allows an input or output to have more than one function)
Bit Grouping	Nonlogic Input/Output	Three State
Buffer	Open Circuit (external resistor)	Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
Compare	Open Circuit (external resistor)	Used for factoring terms using algebraic techniques.
Dynamic	OR	Information not defined.
Exclusive OR	Passive Pull Down (internal resistor)	Logic symbol not defined due to complexity.
Hysteresis	Passive Pull Up (internal resistor)	
Interrogation	Postponed	
Internal Connection	Shift Left (or up)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	-	Count Down


MATH FUNCTIONS

Adder	Greater Than
Arithmetic Logic Unit	Less Than
Comparator	Look Ahead Carry Generator
Divide By	Multiplier
Equal To	Subtractor

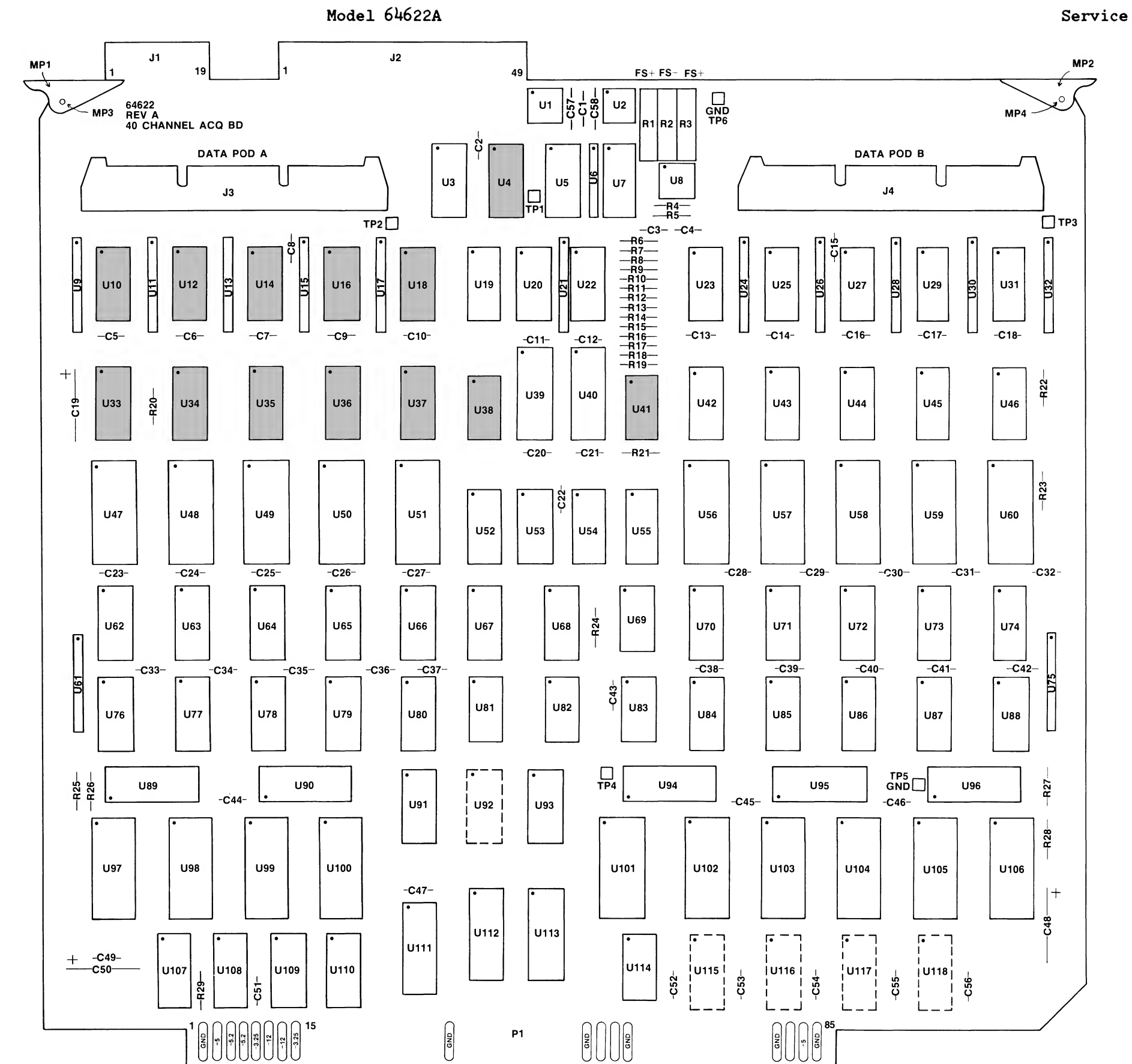
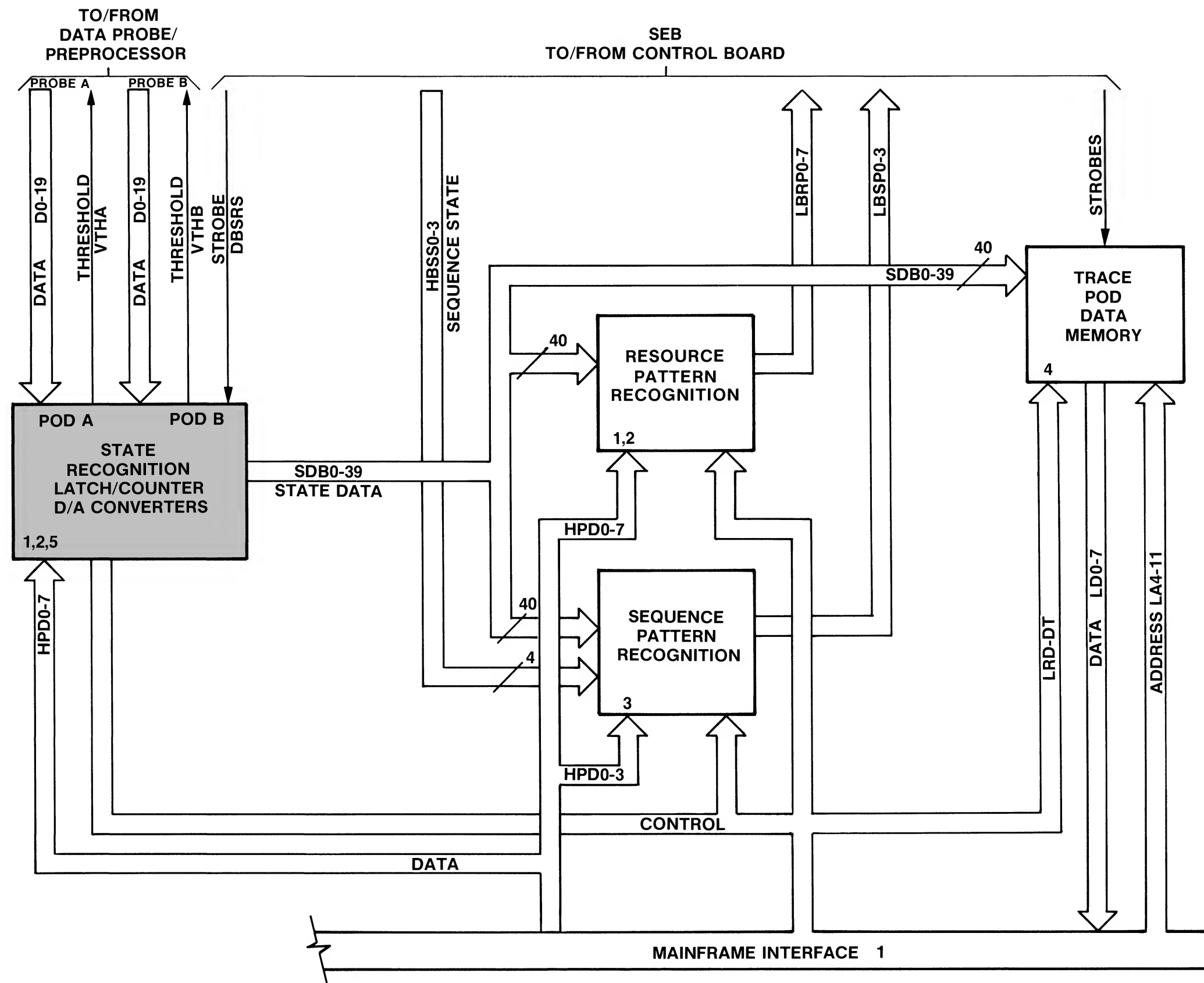
CHIP FUNCTIONS

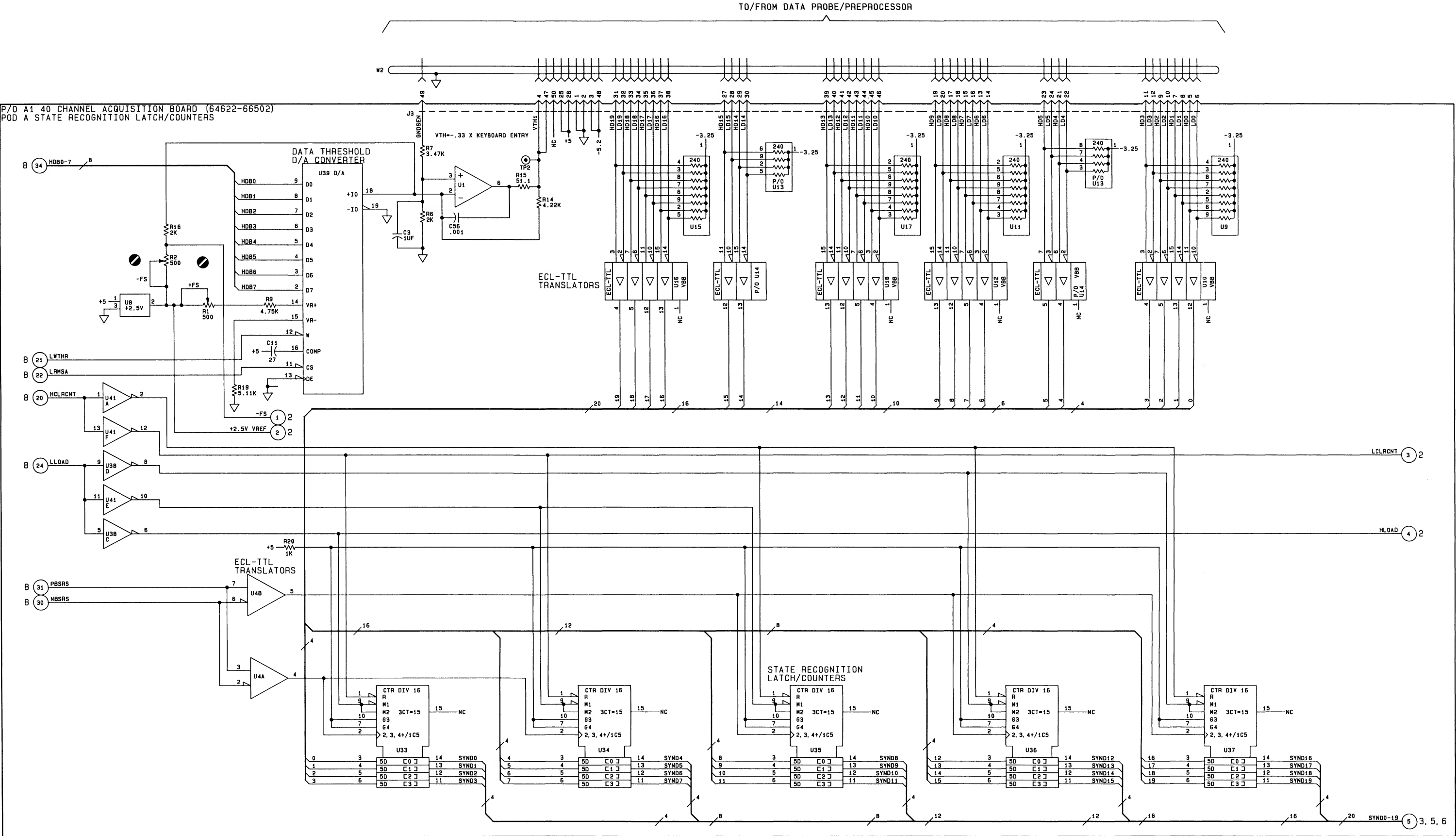
BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

	Astable	NV	Nonvolatile
	Delay	I	State of initial power up
	Nonretriggerable Monostable		Retriggerable Monostable

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ICs ON THIS SCHEMATIC		
Ref. Des.	HP Part No.	Mfr Part No.
U4,10,12, 14,16,18	1820-1052	MC10125L
U33-37	1820-1475	93S16DC
U38,41	1820-1199	SN74LS04N

PARTS ON THIS SCHEMATIC	
C3,11	
J3	
R1,2,6,7,9,14-16,19,20	
TP2	
U1,4,8,9-18,33-39,41	
W2	

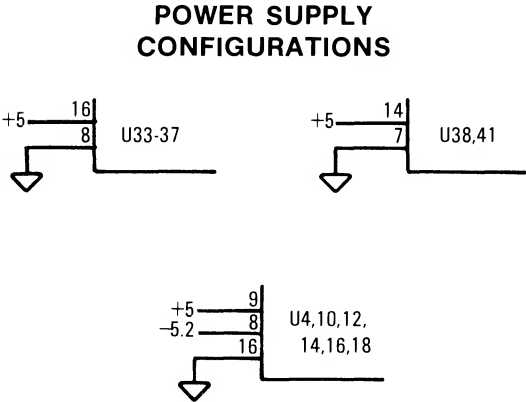
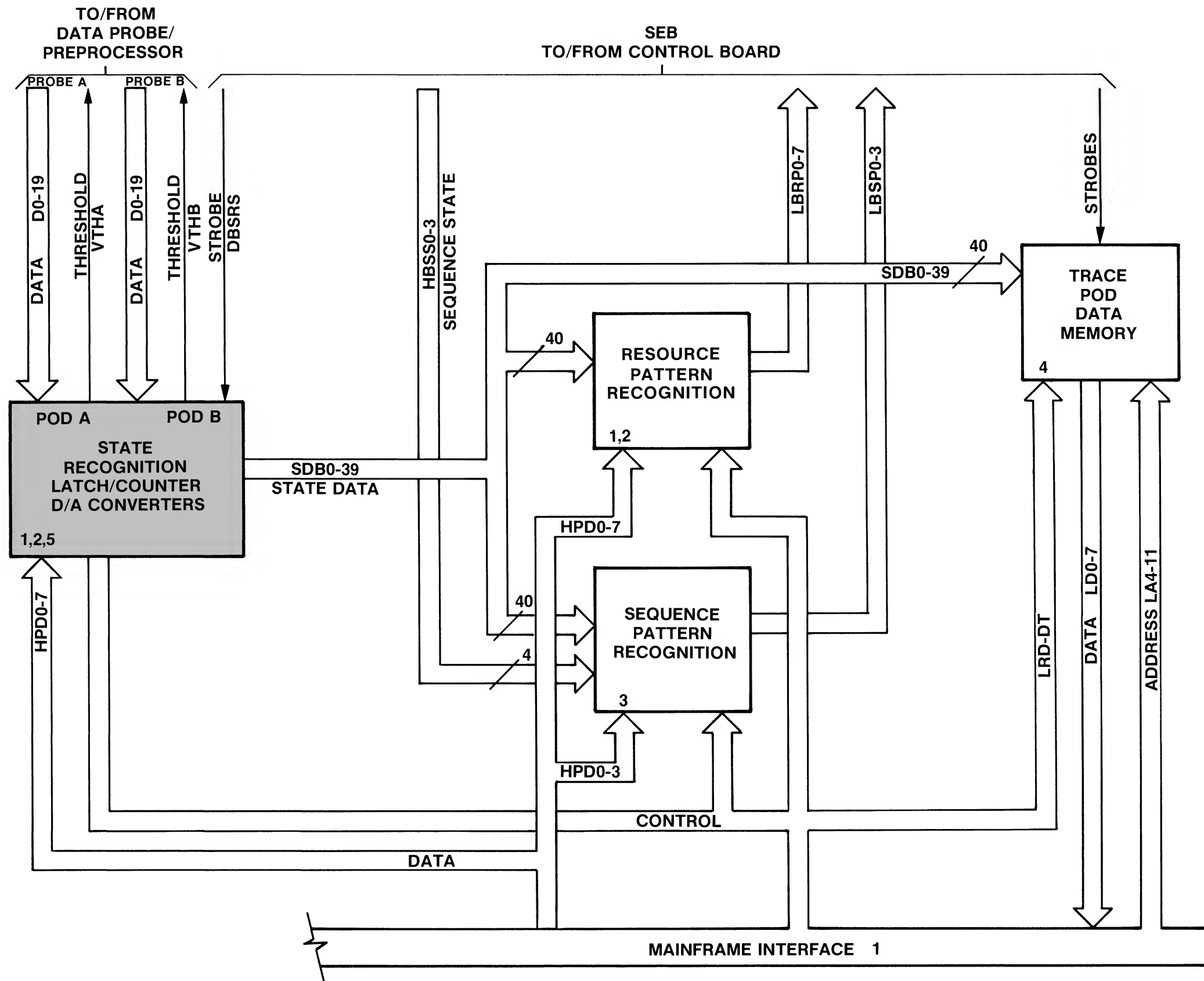


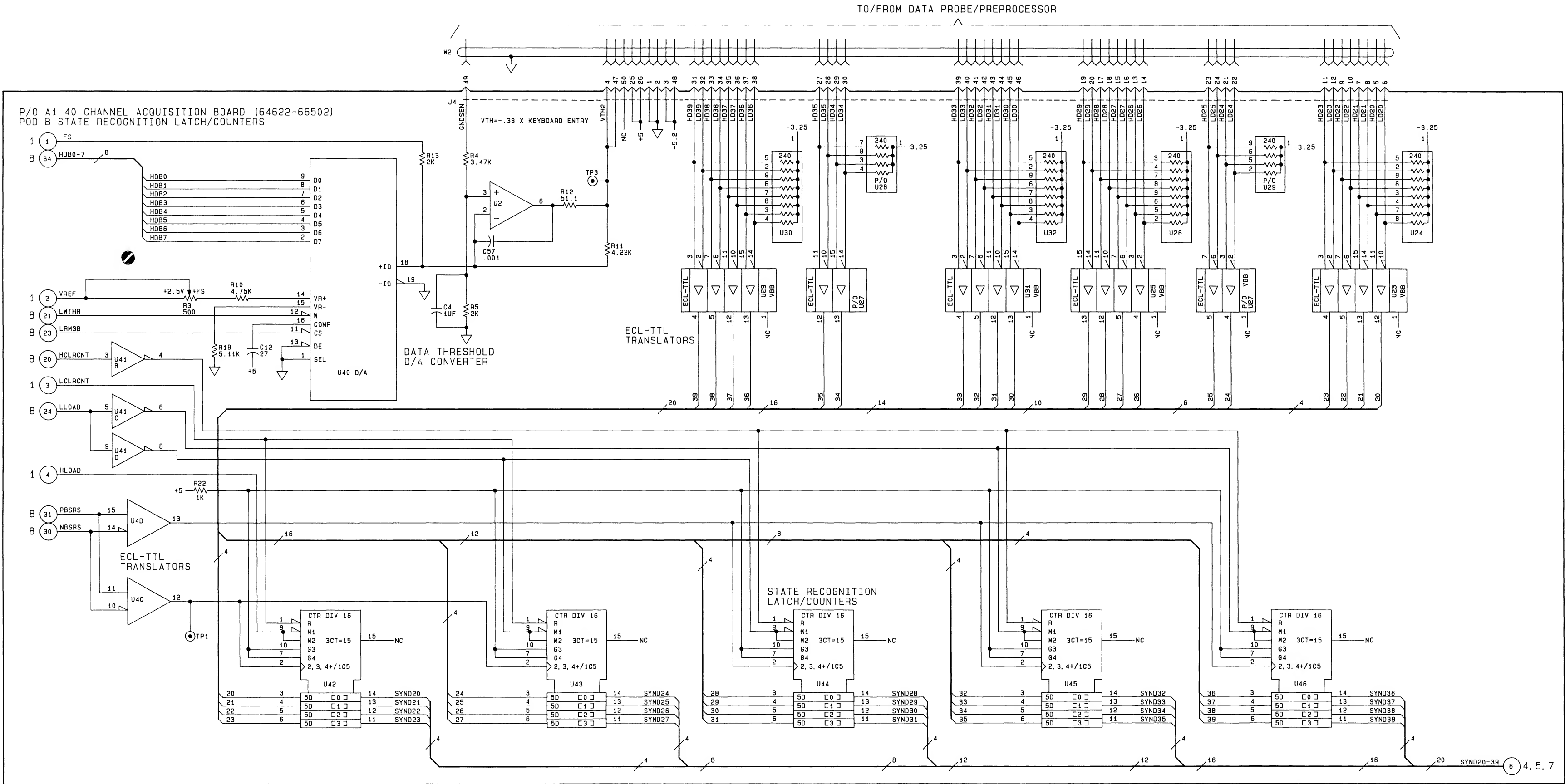
Figure 8-2.
Pod A State Recognition Latch/Counters
40ACQ 8-13

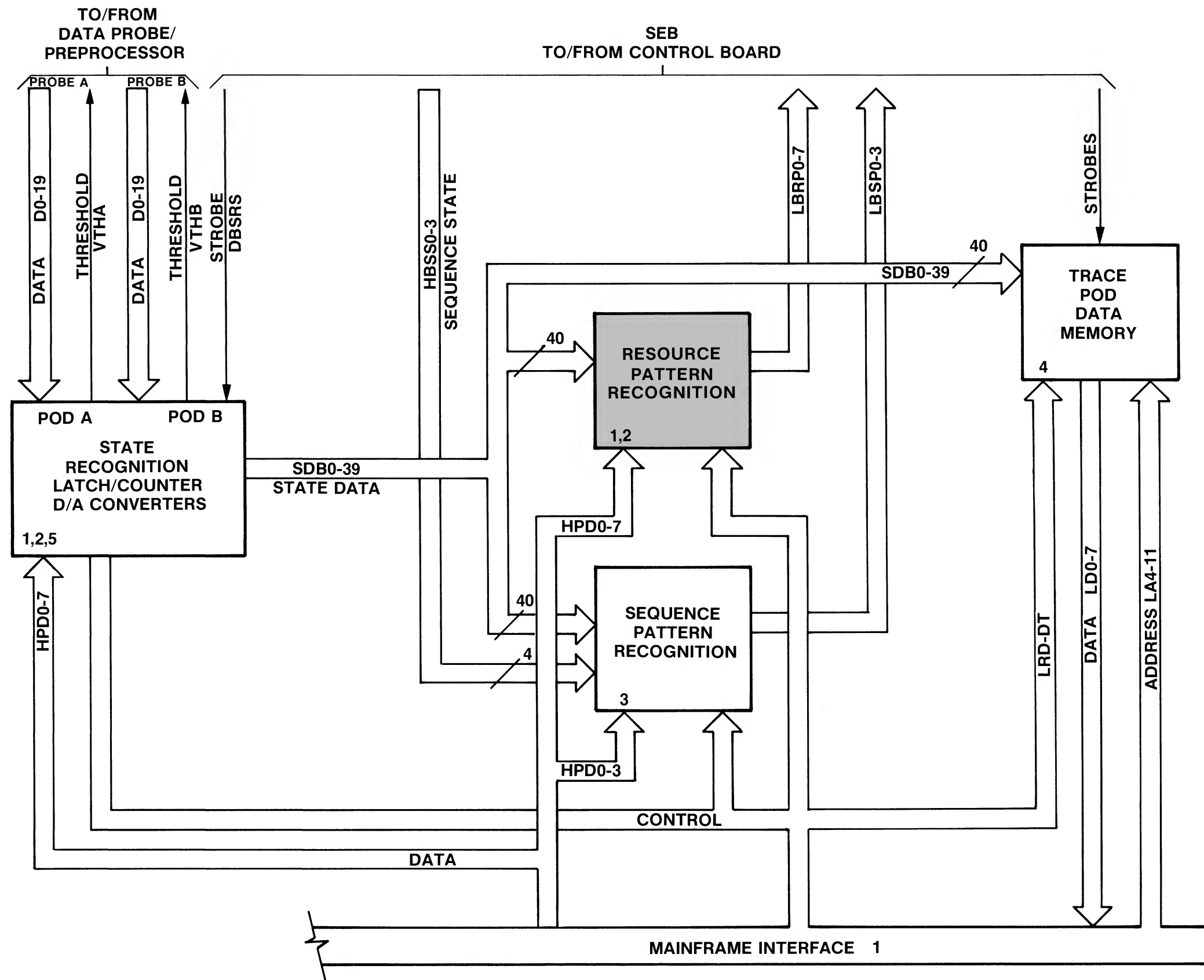


Block Diagram



Component Locator

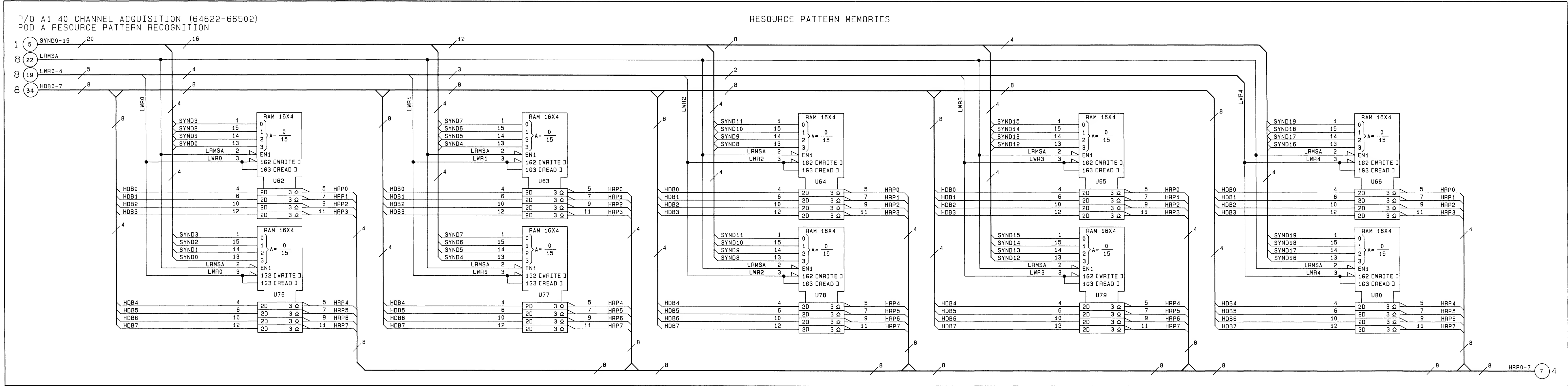


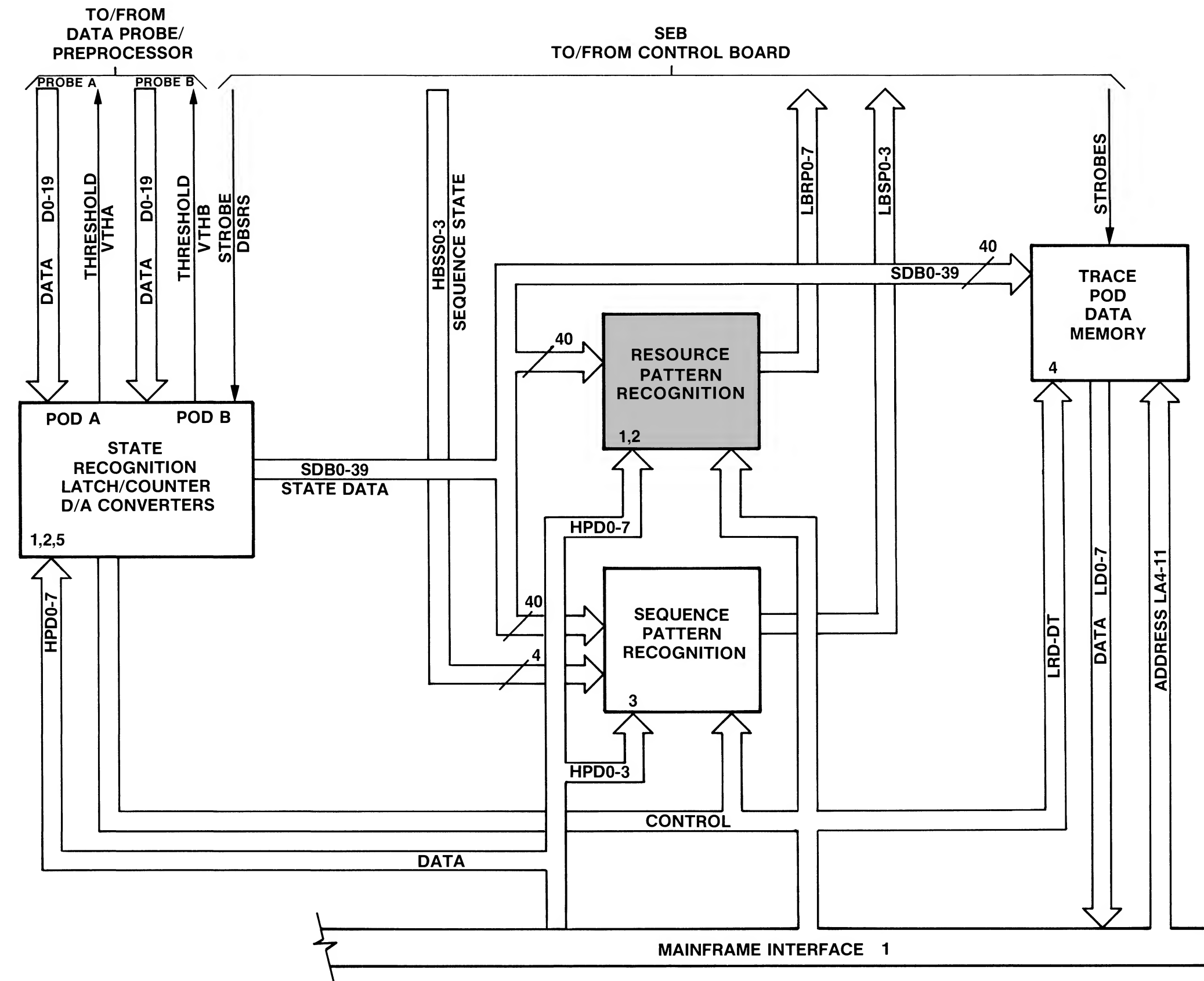


Block Diagram



Component Locator





Block Diagram



Component Locator

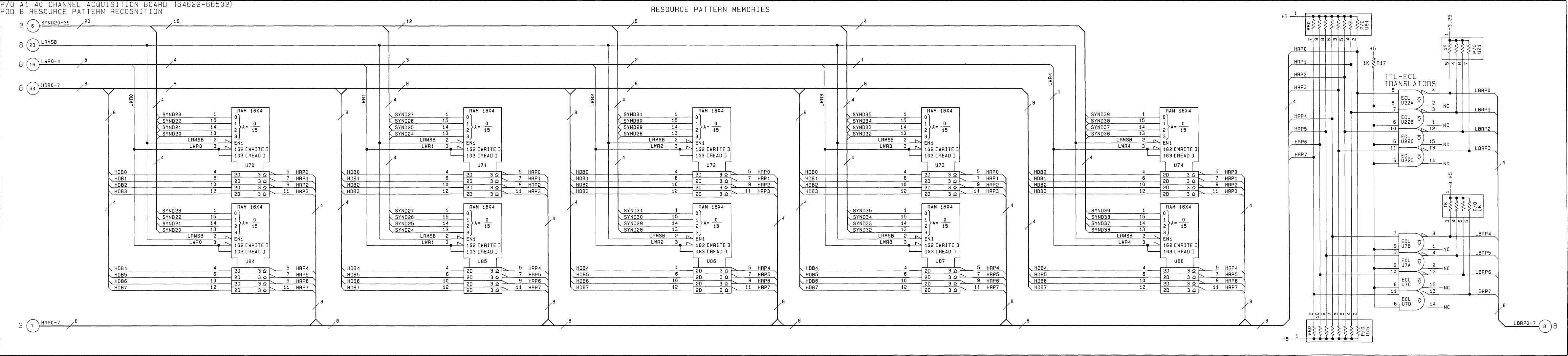
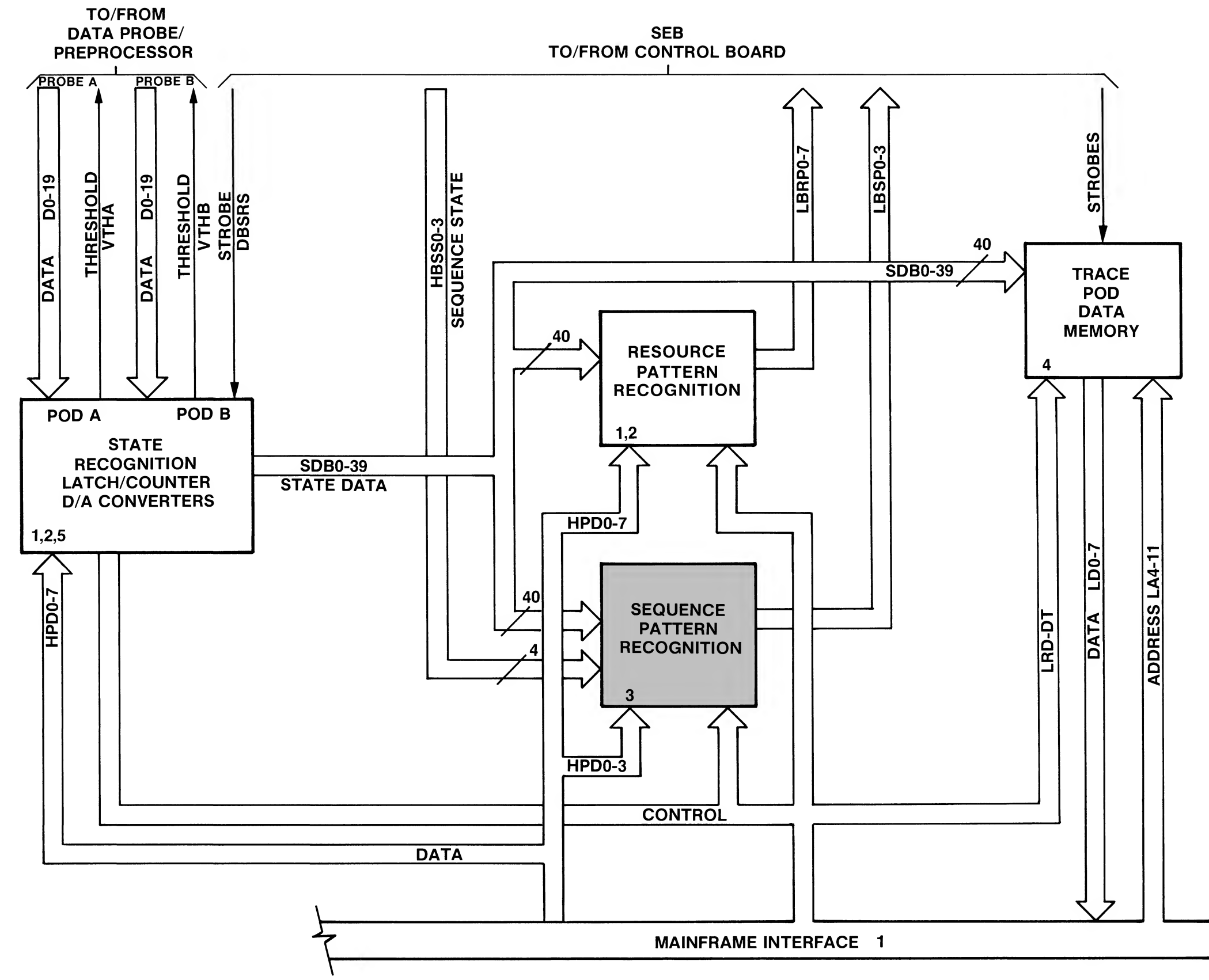


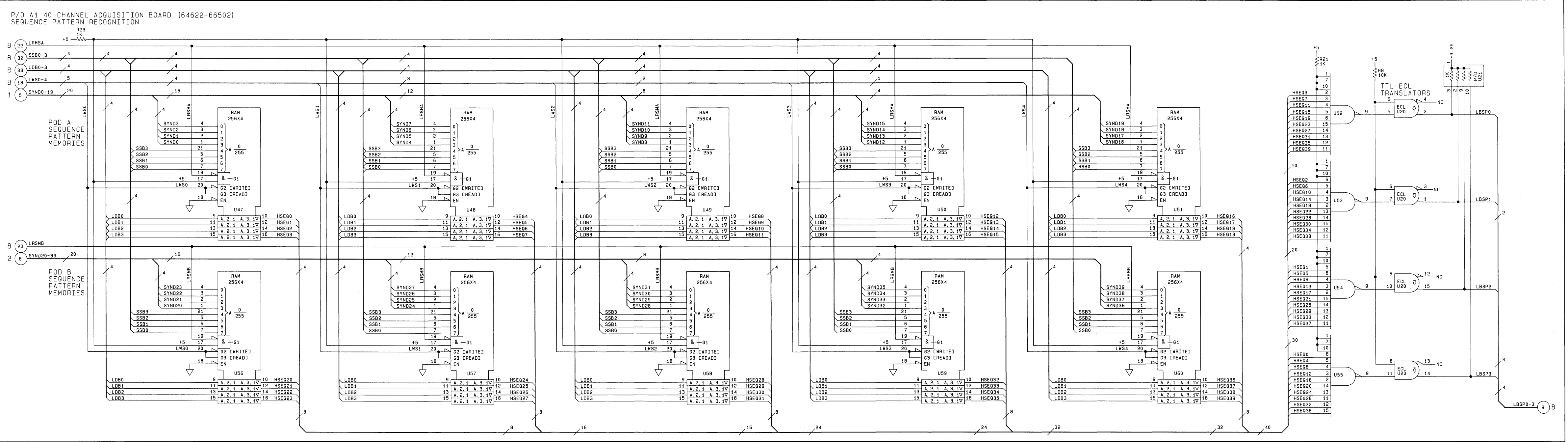
Figure 8-5.
Pod B Resource Pattern Recognition
40ACQ 8-19



Block Diagram



Component Locator



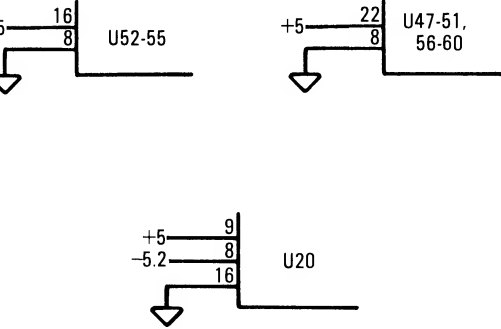
ICs ON THIS SCHEMATIC

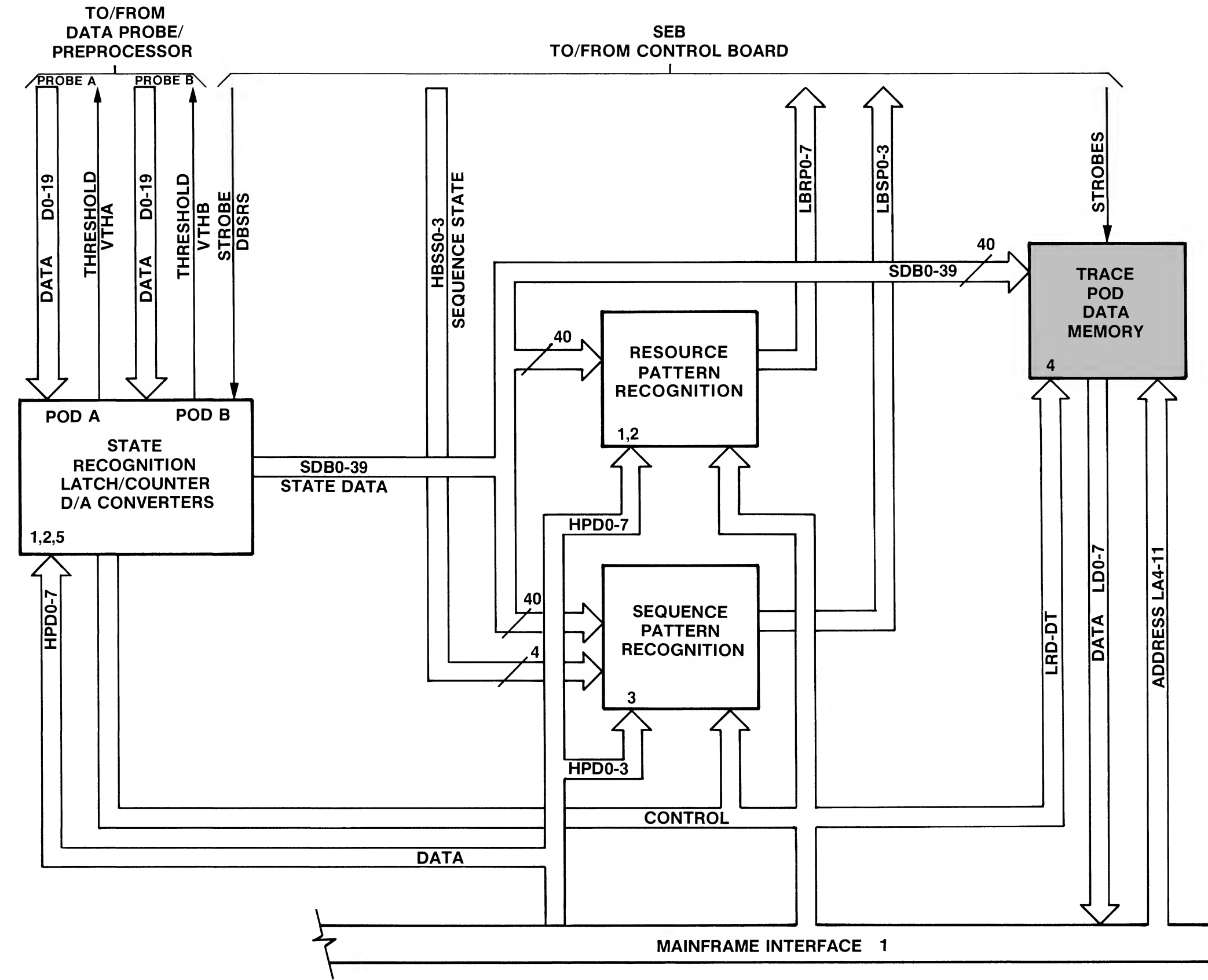
Ref. Des.	HP Part No.	Mfr Part No.
U20	1820-1173	10124
U47-51, 56-60	1816-1476	93L422
U52-55	1820-1130	74LS133

PARTS ON THIS SCHEMATIC

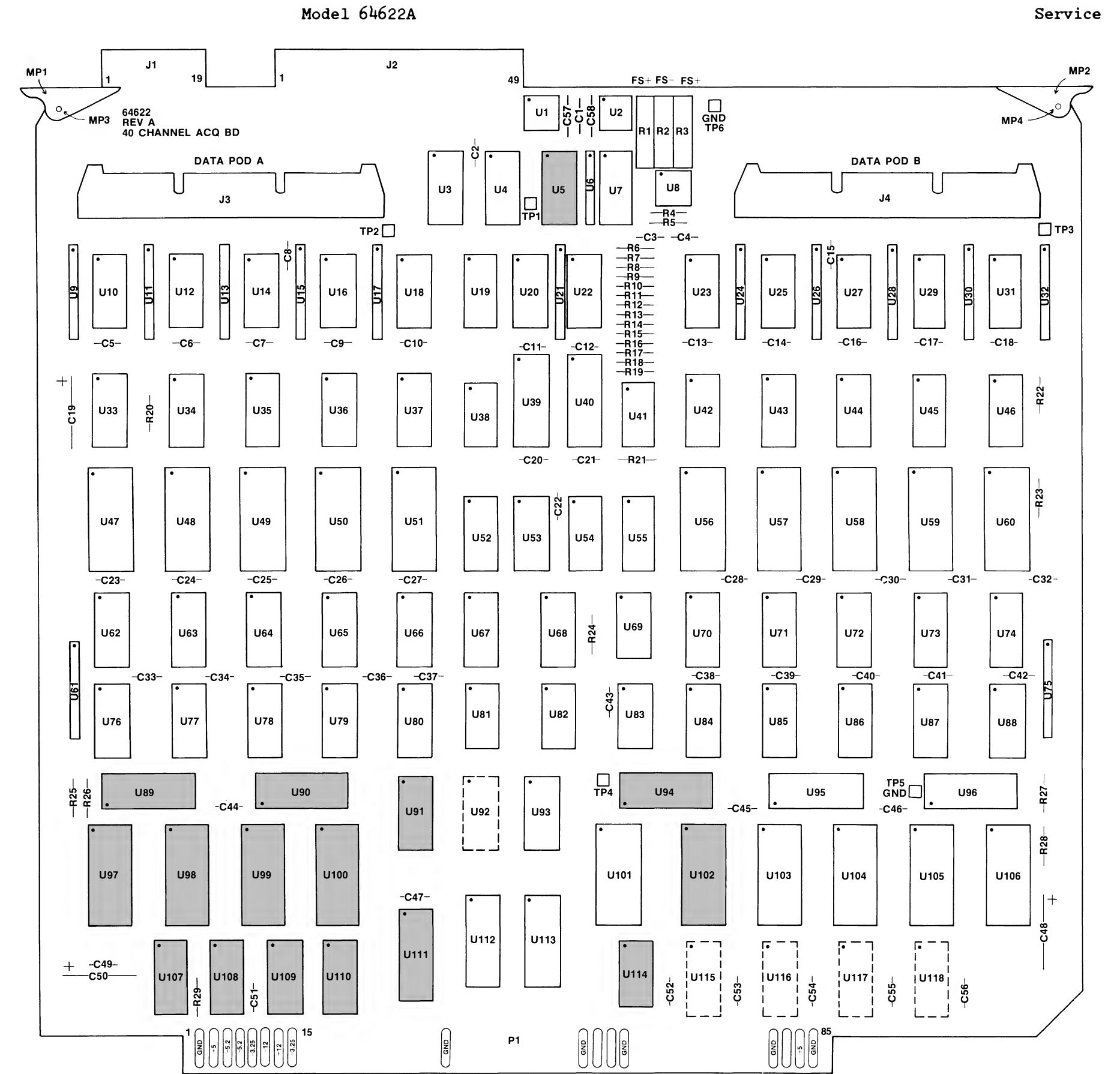
R8,21,23 U20,21,47-60

POWER SUPPLY
CONFIGURATIONS





Block Diagram



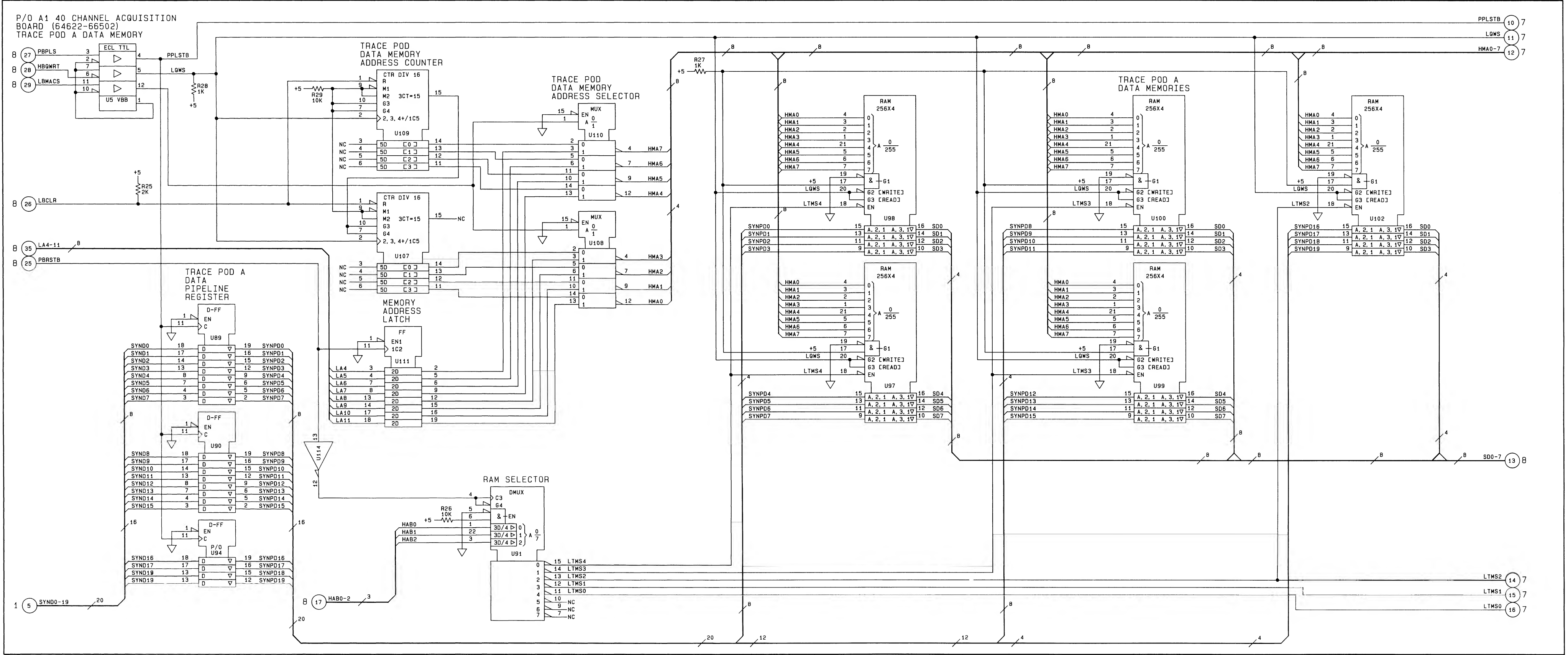
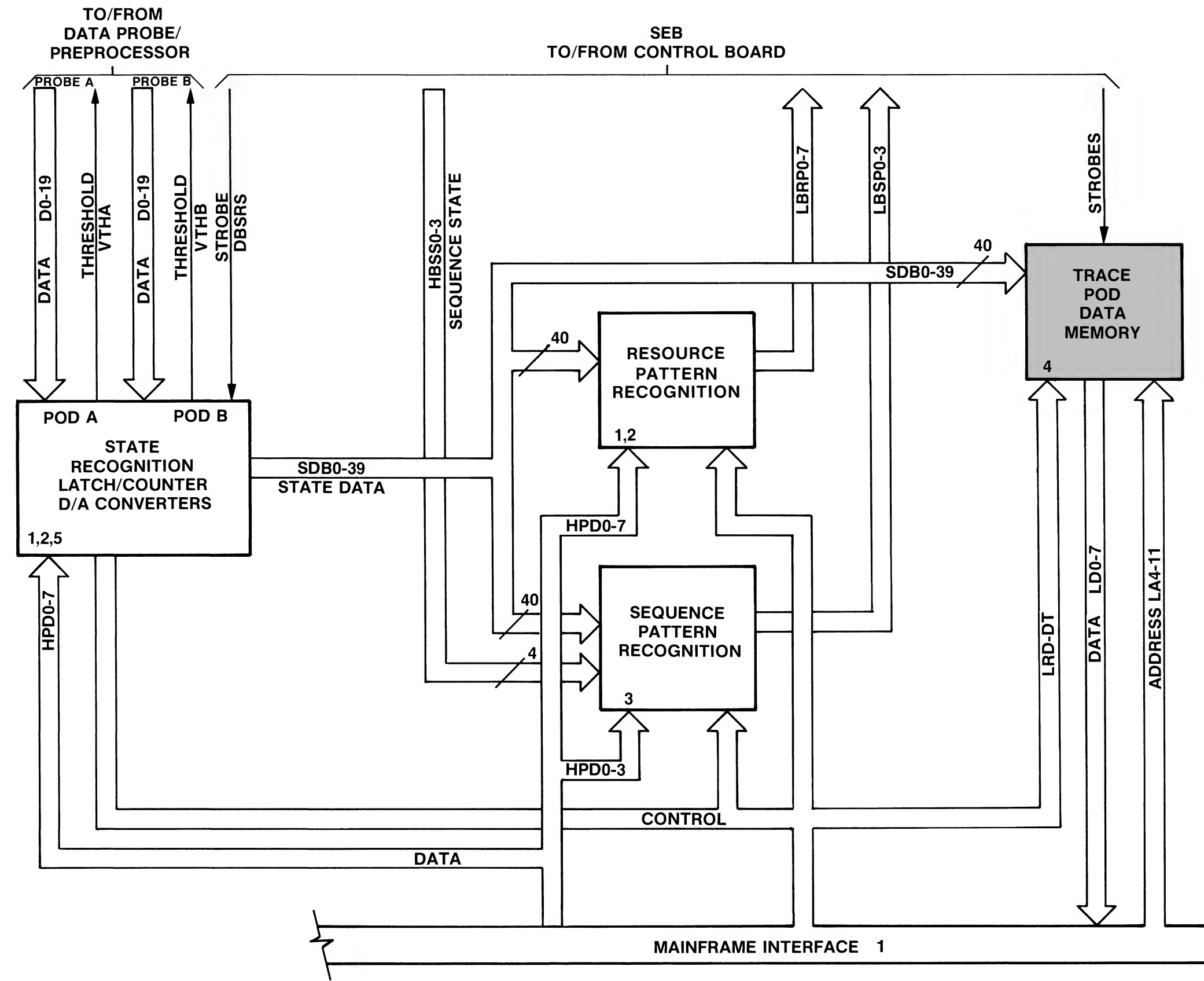
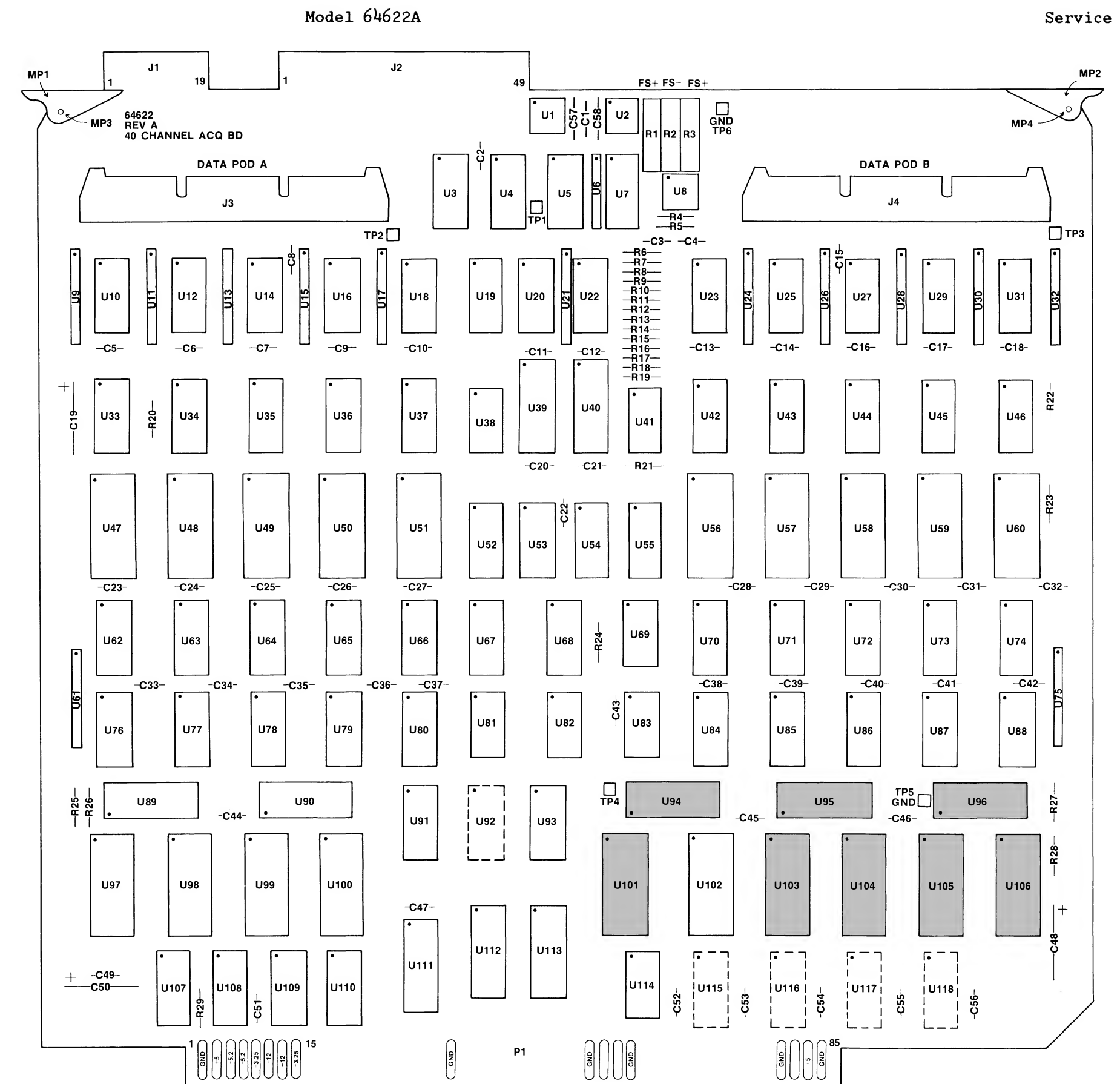


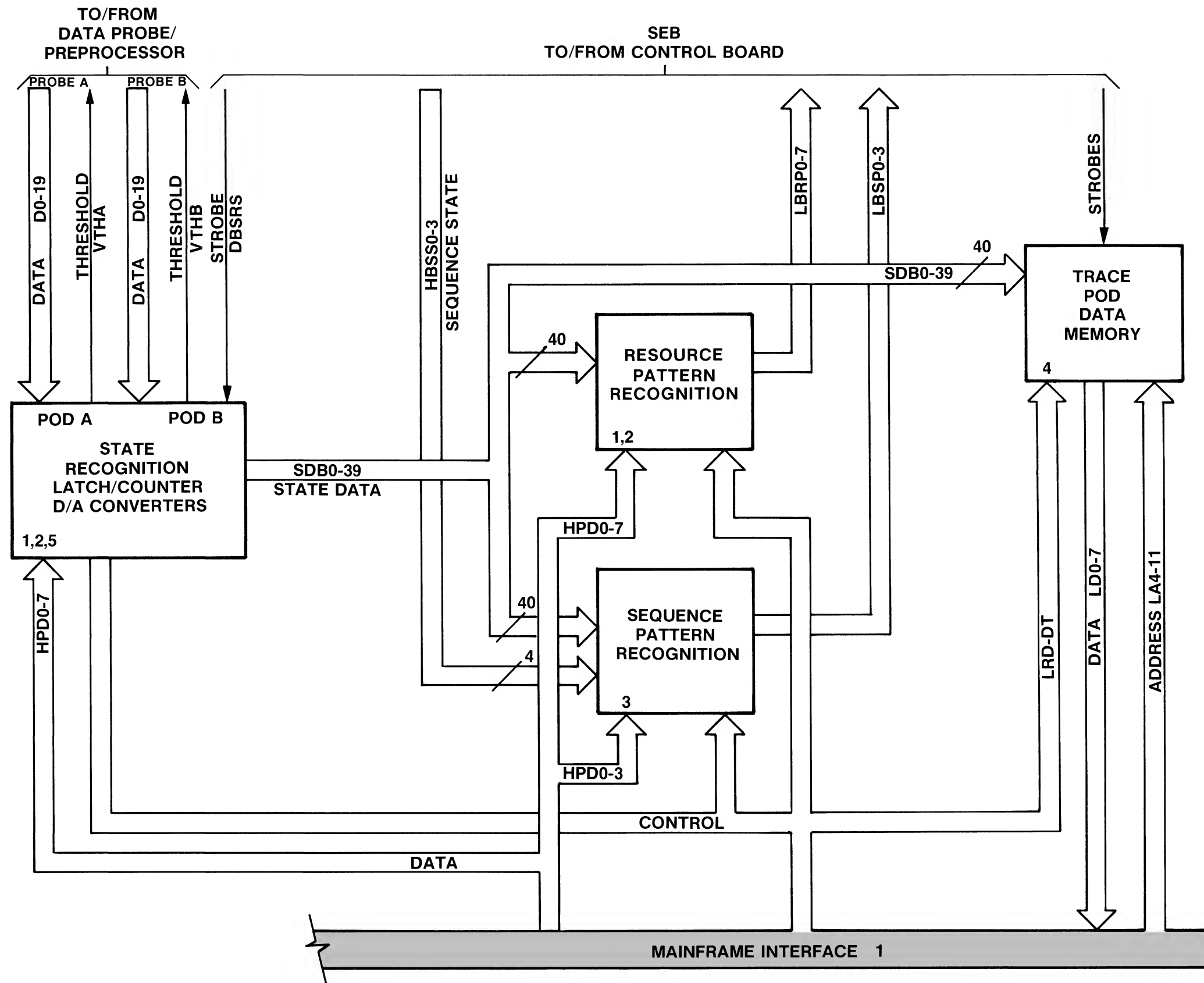
Figure 8-7.
Trace Pod A Data Memory
40ACQ 8-23



Block Diagram



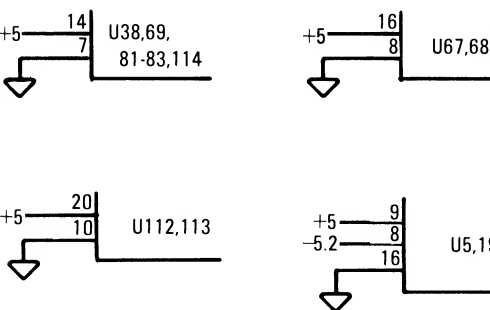
Component Locator



Block Diagram



Component Locator



NOTES

SALES & SUPPORT OFFICES

Arranged alphabetically by country

1



Product Line Sales/Support Key

Key Product Line

- A Analytical
- CM Components
- C Computer Systems Sales only
- CH Computer Systems Hardware Sales and Services
- CS Computer Systems Software Sales and Services
- E Electronic Instruments & Measurement Systems
- M Medical Products
- MP Medical Products Primary SRO
- MS Medical Products Secondary SRO
- P Personal Computation Products
- * Sales only for specific product line
- ** Support only for specific product line

IMPORTANT: These symbols designate general product line capability. They do not insure sales or support availability for all products within a line, at all locations. Contact your local sales office for information regarding locations where HP support is available for specific products.

HP distributors are printed in italics.

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CH-1217 MEYRIN 2, Switzerland
Tel: (022) 83 12 12
Telex: 27835 hpse
Cable: HEWPACKSA Geneve

ASIA

Hewlett-Packard Asia Ltd.
6th Floor, Sun Hung Kai Centre
30 Harbour Rd.
G.P.O. Box 795
HONG KONG
Tel: 5-832 3211
After Jan. 1, 1984
47th Floor, China Resources Bldg.
26 Harbour Rd., Wanchai
HONG KONG
Telex: 66678 HEWPA HX
Cable: HEWPACK HONG KONG

CANADA

Hewlett-Packard (Canada) Ltd.
6877 Goreway Drive
MISSISSAUGA, Ontario L4V 1M8
Tel: (416) 678-9430
Telex: 610-492-4246

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Hewlett-Packard Ges.m.b.h.
Liebigasse 1
P.O. Box 72
A-1222 VIENNA, Austria
Tel: (222) 2365110
Telex: 1 3 4425 HEPA A

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Hewlett-Packard S.A.
Uilenstede 475
P.O. Box 999
NL-1180 AZ AMSTELVEEN
The Netherlands
Tel: 20 437771

SOUTH EAST EUROPE

Hewlett-Packard S.A.
7, Rue du Bois-du-Lan
CH-1217 MEYRIN 2, Switzerland
Tel: (022) 83 12 12
Telex: 27835 hpse
Cable: HEWPACKSA Geneve

OTHER EUROPE

Hewlett-Packard S.A.
P.O. Box
150, Rue du Nant-D'Avril
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Tel: (022) 83 8111
Telex: 22486 hpsa
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32 Kifissias Ave.
Paradissos-Amarousion, ATHENS
Greece
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Telex: 21-6588 HPAT GR
Cable: HEWPACKSA Athens

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4 Choke Cherry Road
ROCKVILLE, MD 20850
Tel: (301) 258-2000

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Hewlett-Packard Co.
5201 Tollview Drive
ROLLING MEADOWS, IL 60008
Tel: (312) 255-9800

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Hewlett-Packard Co.
2000 South Park Place
P.O. Box 105005
ATLANTA, GA 30348
Tel: (404) 955-1500

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Hewlett-Packard Co.
3939 Lankershim Blvd.
P.O. Box 3919
LOS ANGELES, CA 91604
Tel: (213) 506-3700

OTHER INTERNATIONAL AREAS

Hewlett-Packard Co.
Intercontinental Headquarters
3495 Deer Creek Road
PALO ALTO, CA 94304
Tel: (415) 857-1501
Telex: 034-8300
Cable: HEWPACK

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Telectra
Empresa Técnica de Equipamentos
R. Barbosa Rodrigues, 41-I DT.
Caixa Postal 6487
LUANDA
Tel: 355 15, 355 16
E,P

ARGENTINA

Hewlett-Packard Argentina S.A.
Avenida Santa Fe 2035
Martínez 1640 BUENOS AIRES
Tel: 798-5735, 792-1293
Telex: 17595 BIONAR
Cable: HEWPACKARG
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Biotron S.A.C.I.M. e I.
Av Paseo Colon 221, Piso 9
1399 BUENOS AIRES
Tel: 30-4846, 30-1851
Telex: 17595 BIONAR
M

AUSTRALIA

Adelaide, South Australia Office

Hewlett-Packard Australia Ltd.
153 Greenhill Road
PARKSIDE, S.A. 5063
Tel: 272-5911
Telex: 82536
Cable: HEWPAARD Adelaide
A*,CH,CM,,E,MS,P

Brisbane, Queensland Office

Hewlett-Packard Australia Ltd.
10 Payne Road
THE GAP, Queensland 4061
Tel: 30-4133
Telex: 42133
Cable: HEWPAARD Brisbane
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Canberra, Australia

Capital Territory Office
Hewlett-Packard Australia Ltd.
121 Wollongong Street
FYSHWICK, A.C.T. 2609
Tel: 80 4244
Telex: 62650
Cable: HEWPAARD Canberra
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Hewlett-Packard Australia Ltd.
31-41 Joseph Street
BLACKBURN, Victoria 3130
Tel: 895-2895
Telex: 31-024
Cable: HEWPAARD Melbourne
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Hewlett-Packard Australia Ltd.
261 Stirling Highway
CLAREMONT, W.A. 6010
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Cable: HEWPAARD Perth
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Sydney, New South Wales Office

Hewlett-Packard Australia Ltd.
17-23 Talavera Road
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NORTH RYDE, N.S.W. 2113
Tel: 887-1611
Telex: 21561
Cable: HEWPAARD Sydney
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Hewlett-Packard Ges.m.b.h.
Grottenhofstrasse 94
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Tel: (0316) 291 5 66
Telex: 32375
CH,E
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Liebigasse 1
P.O. Box 72
A-1222 VIENNA
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Hewlett-Packard do Brasil I.e.C. Ltda.
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Avenida Epitacio Pessoa, 4664
22471 RIO DE JANEIRO-RJ
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Cable: HEWPACK Rio de Janeiro
A,CH,CM,E,MS,P*
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Rua Bage, 103
04012 SAO PAULO
Tel: (011) 570-5726
Telex: 021-21905 HPBR-BR
M



SALES & SUPPORT OFFICES

Arranged alphabetically by country

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Hewlett-Packard (Canada) Ltd.
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Tel: (403) 235-3100
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EDMONTON, Alberta T5S 1P2
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Boite Postale 162
F-69130 ECULLY Cedex (Lyon)
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Telex: 310617F
A,CH,CS,E,MP

Hewlett-Packard France
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Boulevard de France
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Tel: 16 6 077-96-60
Telex: 692315F
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Hewlett-Packard France
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Tel: 16 6 077-8383
Telex: 692315F
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Hewlett-Packard France
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Bâtiment Ampère 5 étage
Rue de la Commune de Paris
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Telex: 211032F
CH,CS,E,MS

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Parc d'Activités Caderea
Quartier Jean Mermoz
Avenue du Président JF Kennedy
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Telex: 550105F
CH,E,MS

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Hewlett-Packard France
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Tel: 16 (38) 68 01 63

Hewlett-Packard France
Zone Industrielle de Courtaboeuf
Avenue des Tropiques
F-91947 Les Ulis Cedex ORSAY
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A,CH,CM,CS,E,MP,P

Hewlett-Packard France
Paris Porte-Maillet
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F-75782 PARIS CEDEX 16
Tel: 16 (1) 502-12-20
Telex: 613663F
CH,MS,P

Hewlett-Packard France
124, Boulevard Tourasse
F-64000 PAU
Tel: 16 (59) 80 38 02

Hewlett-Packard France
2 Allée de la Bourgonnette
F-35100 RENNES
Tel: 16 (99) 51-42-44
Telex: 740912F
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Hewlett-Packard France
98 Avenue de Bretagne
F-76100 ROUEN
Tel: 16 (35) 63-57-66
CH*,CS

Hewlett-Packard France
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Boite Postale 56
F-67033 STRASBOURG Cedex
Tel: 16 (88) 28-56-46
Telex: 890141F
CH,E,MS,P*

Hewlett-Packard France
Le Péripole
20, Chemin du Pigeonnier de la
Cépière
F-31083 TOULOUSE Cedex
Tel: 16 (61) 40-11-12
Telex: 531639F
A,CH,CS,E,P*

Hewlett-Packard France
9, rue Baudin
F-26000 VALENCE
Tel: 16 (75) 42 76 16

Hewlett-Packard France
Carolor
ZAC de Bois Briand
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Tel: 16 (8) 771 20 22
CH

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F-59658 VILLENEUVE D'ASCO Cedex
Tel: 16 (20) 91-41-25
Telex: 160124F
CH,E,MS,P*

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Hewlett-Packard GmbH
Geschäftsstelle
Keithstrasse 2-4
D-1000 BERLIN 30
Tel: (030) 24-90-86
Telex: 018 3405 hpbln d
A,CH,E,M,P

Hewlett-Packard GmbH
Geschäftsstelle
Herrenberger Strasse 130
D-7030 BOBLINGEN
Tel: (7031) 14-0
Telex:
A,CH,CM,CS,E,MP,P

Hewlett-Packard GmbH
Geschäftsstelle
Emanuel-Leutze-Strasse 1
D-4000 DUSSELDORF
Tel: (0211) 5971-1
Telex: 085/86 533 hpdd d
A,CH,CS,E,MS,P

Hewlett-Packard GmbH
Geschäftsstelle
Schleefstr. 28a
D-4600 DORTMUND-Aplerbeck
Tel: (0231) 45001

Hewlett-Packard GmbH
Vertriebszentrale Frankfurt
Bernier Strasse 117
Postfach 560 140
D-6000 FRANKFURT 56
Tel: (0611) 50-04-1
Telex: 04 13249 hpffm d
A,CH,CM,CS,E,MP,P

Hewlett-Packard GmbH
Geschäftsstelle
Aussenstelle Bad Homburg
Louisenstrasse 115
D-6380 BAD HOMBURG
Tel: (06172) 109-0

Hewlett-Packard GmbH
Geschäftsstelle
Kapstadtring 5
D-2000 HAMBURG 60
Tel: (040) 63804-1
Telex: 021 63 032 hphh d
A,CH,CS,E,MS,P

Hewlett-Packard GmbH
Geschäftsstelle
Heidering 37-39
D-3000 HANNOVER 61
Tel: (0511) 5706-0
Telex: 092 3259
A,CH,CM,E,MS,P

Hewlett-Packard GmbH
Geschäftsstelle
Rosslauer Weg 2-4
D-6800 MANNHEIM
Tel: (0621) 70050
Telex: 0462105
A,C,E

Hewlett-Packard GmbH
Geschäftsstelle
Messerschmittstrasse 7
D-7910 NEU ULM
Tel: 0731-70241
Telex: 0712816 HP ULM-D
A,C,E*

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Geschäftsstelle
Ehrlicherstr. 13
D-8500 NÜRNBERG 10
Tel: (0911) 5205-0
Telex: 0623 860
CH,CM,E,MS,P

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Geschäftsstelle
Eschenstrasse 5
D-8028 TAUFKIRCHEN
Tel: (089) 6117-1
Telex: 0524985
A,CH,CM,E,MS,P

GREAT BRITAIN

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GREECE

Kostas Karaynnis S.A.
8 Omirou Street
ATHENS 133
Tel: 32 30 303, 32 37 371
Telex: 215962 RKAR GR
A,CH,CM,CS,E,M,P

PLAISIO S.A.
G. Gerardos
24 Stournara Street
ATHENS
Tel: 36-11-160
Telex: 221871
P

GUATEMALA

IPESA
Avenida Reforma 3-48, Zona 9
GUATEMALA CITY
Tel: 316627, 314786
Telex: 4192 TELTRO GU
A,CH,CM,CS,E,M,P

HONG KONG

Hewlett-Packard Hong Kong, Ltd.
G.P.O. Box 795
5th Floor, Sun Hung Kai Centre
30 Harbour Road
HONG KONG
Tel: 5-8323211
Telex: 66678 HEWPA HX
Cable: HEWPACK HONG KONG
E,CH,CS,P

CET Ltd.
1402 Tung Wah Mansion
199-203 Hennessy Rd.
Wanchia, HONG KONG
Tel: 5-729376
Telex: 85148 CET HX
CM

Schmidt & Co. (Hong Kong) Ltd.
Wing On Centre, 28th Floor
Connaught Road, C.
HONG KONG
Tel: 5-455644
Telex: 74766 SCHMX HX
A,M

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Hafnarnvöli-Tryggvagotu
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IS-REYKJAVIK
Tel: 1-58-20, 1-63-03
M

INDIA

Computer products are sold through
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Blue Star Ltd.
Sabri Complex II Floor
24 Residency Rd.
BANGALORE 560 025
Tel: 55660
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Cable: BLUESTAR
A,CH*,CM,CS*,E

Blue Star Ltd.
Band Box House
Prabhadevi
BOMBAY 400 025
Tel: 422-3101
Telex: 011-3751
Cable: BLUESTAR
A,M

Blue Star Ltd.
Sahas
414/2 Vir Savarkar Marg
Prabhadevi
BOMBAY 400 025
Tel: 422-6155
Telex: 011-4093
Cable: FROSTBLUE
A,CH*,CM,CS*,E,M

Blue Star Ltd.
Kalyan, 19 Vishwas Colony
Alkapuri, BORODA, 390 005
Tel: 65235
Cable: BLUE STAR
A

Blue Star Ltd.
7 Hare Street
CALCUTTA 700 001
Tel: 12-01-31
Telex: 021-7655
Cable: BLUESTAR
A,M

Blue Star Ltd.
133 Kodambakkam High Road
MADRAS 600 034
Tel: 82057
Telex: 041-379
Cable: BLUESTAR
A,M

Blue Star Ltd.
Bhandari House, 7th/8th Floors
91 Nehru Place
NEW DELHI 110 024
Tel: 682547
Telex: 031-2463
Cable: BLUESTAR
A,CH*,CM,CS*,E,M

Blue Star Ltd.
15/16-C Wellesley Rd.
PUNE 411 011
Tel: 22775
Cable: BLUE STAR
A

Blue Star Ltd.
2-2-47/1108 Bolarum Rd.
SECUNDERABAD 500 003
Tel: 72057
Telex: 0155-459
Cable: BLUEFROST
A,E

Blue Star Ltd.
T.C. 7/603 Poornima
Maruthankuzhi
TRIVANDRUM 695 013
Tel: 65799
Telex: 0884-259
Cable: BLUESTAR
E

Computer Maintenance Corporation
Ltd.
115, Sarojini Devi Road
SECUNDERABAD 500 003
Tel: 310-184, 345-774
Telex: 031-2960
CH**



SALES & SUPPORT OFFICES

Arranged alphabetically by country

INDONESIA

BERCA Indonesia P.T.
P.O.Box 496/Jkt.
Jl. Abdul Muis 62
JAKARTA
Tel: 21-373009
Telex: 46748 BERSAL IA
Cable: BERSAL JAKARTA
P

BERCA Indonesia P.T.
P.O.Box 2497/Jkt
Antara Bldg., 17th Floor
Jl. Medan Merdeka Selatan 17
JAKARTA-PUSAT
Tel: 21-344-181
Telex: BERSAL IA
A,CS,E,M

BERCA Indonesia P.T.
P.O. Box 174/SBY.
Jl. Kutei No. 11
SURABAYA
Tel: 68172
Telex: 31146 BERSAL SB
Cable: BERSAL-SURABAYA
A*,E,M,P

IRAQ

Hewlett-Packard Trading S.A.
Service Operation
Al Mansoor City 9B/3/7
BAGHDAD
Tel: 551-49-73
Telex: 212-455 HEPARQA IK
CH,CS

IRELAND

Hewlett-Packard Ireland Ltd.
82/83 Lower Leeson Street
DUBLIN 2
Tel: 0001 608800
Telex: 30439
A,CH,CM,CS,E,M,P
Cardiac Services Ltd.
Kilmore Road
Artane
DUBLIN 5
Tel: (01) 351820
Telex: 30439
M

ISRAEL

Eidan Electronic Instrument Ltd.
P.O.Box 1270
JERUSALEM 91000
16, Ohaliav St.
JERUSALEM 94467
Tel: 533 221, 553 242
Telex: 25231 AB/PAKRD IL
A

Electronics Engineering Division
Motorola Israel Ltd.
16 Kremenetski Street
P.O. Box 25016
TEL-AVIV 67899
Tel: 3 88 388
Telex: 33569 Motil IL
Cable: BASTEL Tel-Aviv
CH,CM,CS,E,M,P

ITALY

Hewlett-Packard Italiana S.p.A.
Traversa 99C
Via Giulio Petroni, 19
I-70124 **BARI**
Tel: (080) 41-07-44
M

Hewlett-Packard Italiana S.p.A.
Via Martin Luther King, 38/III
I-40132 **BOLOGNA**
Tel: (051) 402394
Telex: 511630
CH,E,MS

Hewlett-Packard Italiana S.p.A.
Via Principe Nicola 43G/C
I-95126 **CATANIA**
Tel: (095) 37-10-87
Telex: 970291
C,P

Hewlett-Packard Italiana S.p.A.
Via G. Di Vittorio 9
I-20063 **CERNUSCO SUL NAVIGLIO**
(Milano)
Tel: (02) 923691
Telex: 334632
A,CH,CM,CS,E,MP,P
Hewlett-Packard Italiana S.p.A.
Via C. Colombo 49
I-20090 **TREZZANO SUL NAVIGLIO**
(Milano)
Tel: (02) 4459041
Telex: 322116
C,M

Hewlett-Packard Italiana S.p.A.
Via Nuova San Rocco a
Capodimonte, 62/A
I-80131 **NAPOLI**
Tel: (081) 7413544
Telex: 710698
A,CH,E

Hewlett-Packard Italiana S.p.A.
Viale G. Modugno 33
I-16156 **GENOVA PEGLI**
Tel: (010) 68-37-07
Telex: 215238
E,C

Hewlett-Packard Italiana S.p.A.
Via Pelizzo 15
I-35128 **PADOVA**
Tel: (049) 664888
Telex: 430315
A,CH,E,MS

Hewlett-Packard Italiana S.p.A.
Viale C. Pavese 340
I-00144 **ROMA EUR**
Tel: (06) 54831
Telex: 610514
A,CH,CM,CS,E,MS,P*

Hewlett-Packard Italiana S.p.A.
Via di Casellina 57/C
I-50018 **SCANDICCI-FIRENZE**
Tel: (055) 753863

Hewlett-Packard Italiana S.p.A.
Corso Svizzera, 185
I-10144 **TORINO**
Tel: (011) 74 4044
Telex: 221079
CH,E

JAPAN

Hewlett-Packard-Hewlett-Packard Ltd.
152-1, Onna
ATSUGI, Kanagawa, 243
Tel: (0462) 28-0451
CM,C*,E

Yokogawa-Hewlett-Packard Ltd.
Meiji-Seimei Bldg. 6F
3-1 Hon Chiba-Cho
CHIBA, 280
Tel: 472 25 7701
E,CH,CS

Yokogawa-Hewlett-Packard Ltd.
Yasuda-Seimei Hiroshima Bldg.
6-11, Hon-dori, Naka-ku
HIROSHIMA, 730
Tel: 82-241-0611

Yokogawa-Hewlett-Packard Ltd.
Towa Building
2-3, Kaigan-dori, 2 Chome Chuo-ku
KOBE, 650
Tel: (078) 392-4791
C,E

Yokogawa-Hewlett-Packard Ltd.
Kumagaya Asahi 82 Bldg
3-4 Tsukuba
KUMAGAYA, Saitama 360
Tel: (0485) 24-6563
CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
Asahi Shinbun Daiichi Seimei Bldg.
4-7, Hanabata-cho
KUMAMOTO, 860
Tel: (0963) 54-7311
CH,E

Yokogawa-Hewlett-Packard Ltd.
Shin-Kyoto Center Bldg.
614, Higashi-Shiokoji-cho
Karasuma-Nishiiru
Shiokoji-dori, Shimogyo-ku
KYOTO, 600
Tel: 075-343-0921
CH,E

Yokogawa-Hewlett-Packard Ltd.
Mito Mitsui Bldg
4-73, Sanno-maru, 1 Chome
MITO, Ibaraki 310
Tel: (0292) 25-7470
CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
Sumitomo Seimei 14-9 Bldg.
Meiki-Minami, 2 Chome
Nakamura-ku
NAGOYA, 450
Tel: (052) 571-5171
CH,CM,CS,E,MS

Yokogawa-Hewlett-Packard Ltd.
Chuo Bldg.,
4-20 Nishinakajima, 5 Chome
Yodogawa-ku
OSAKA, 532
Tel: (06) 304-6021
Telex: YHPOSA 523-3624
A,CH,CM,CS,E,MP,P*

Yokogawa-Hewlett-Packard Ltd.
27-15, Yabe, 1 Chome
SAGAMIHARA Kanagawa, 229
Tel: 0427 59-1311

Yokogawa-Hewlett-Packard Ltd.
Daiichi Seimei Bldg.
7-1, Nishi Shinjuku, 2 Chome
Shinjuku-ku, **TOKYO** 160
Tel: 03-348-4611
CH,E

Yokogawa-Hewlett-Packard Ltd.
29-21 Takaido-Higashi, 3 Chome
Suginami-ku **TOKYO** 168
Tel: (03) 331-611
Telex: 232-2024 YHPTOK
A,CH,CM,CS,E,MP,P*

Yokogawa-Hewlett-Packard Ltd.
Daiichi Asano Building
2-8, Odori, 5 Chome
UTSUNOMIYA, Tochigi 320
Tel: (0286) 25-7155
CH,CS,E

Yokogawa-Hewlett-Packard Ltd.
Yasuda Seimei Nishiguchi Bldg.
30-4 Tsuruya-cho, 3 Chome
YOKOHAMA 221
Tel: (045) 312-1252
CH,CM,E

JORDAN

Mouasher Cousins Company
P.O. Box 1387
AMMAN
Tel: 24907, 39907
Telex: 21456 SABCO JO
CH,E,M,P

KENYA

ADCOM Ltd., Inc., Kenya
P.O. Box 30070
NAIROBI
Tel: 331955
Telex: 22639
E,M

KOREA

Samsung Electronics HP Division
12 Fl. Kinam Bldg.
San 75-31, Yeoksam-Dong
Kangnam-Ku
Yeongdong P.O. Box 72
SEOUL
Tel: 555-7555, 555-5447
Telex: K27364 SAMSAN
A,CH,CM,CS,E,M,P

KUWAIT

Al-Khaldiya Trading & Contracting
P.O. Box 830 Safat
KUWAIT
Tel: 42-4910, 41-1726
Telex: 22481 Areeg kt
CH,E,M

Photo & Cine Equipment
P.O. Box 270 Safat
KUWAIT
Tel: 42-2846, 42-3801
Telex: 22247 Matin kt
P

LEBANON

G.M. Dolmadjian
Achrafieh
P.O. Box 165. 167
BEIRUT
Tel: 290293
MP**

Computer Information Systems
P.O. Box 11-6274
BEIRUT
Tel: 89 40 73
Telex: 22259
C

LUXEMBOURG

Hewlett-Packard Belgium S.A./N.V.
Blvd de la Woluwe, 100
Woluwedal
B-1200 **BRUSSELS**
Tel: (02) 762-32-00
Telex: 23-494 paloben bru
A,CH,CM,CS,E,MP,P

MALAYSIA

Hewlett-Packard Sales (Malaysia)
Sdn. Bhd.
1st Floor, Bangunan British
American
Jalan Semantan, Damansara Heights
KUALA LUMPUR 23-03
Tel: 943022
Telex: MA31011
A,CH,E,M,P*

SALES & SUPPORT OFFICES

Arranged alphabetically by country

5



MAYLAISIA (Cont'd)

Protel Engineering
P.O. Box 1917
Lot 6624, Section 64
23/4 Pending Road
Kuching, SARAWAK
Tel: 36299
Telex: MA 70904 PROMAL
Cable: PROTELENG
A,E,M

MALTA

Philip Toledo Ltd.
Notabile Rd.
MIRIEHEL
Tel: 447 47, 455 66
Telex: Media MW.649
E,P

MEXICO

Hewlett-Packard Mexicana, S.A.
de C.V.
Av. Periferico Sur No. 6501
Tepepan, Xochimilco
16020 MEXICO D.F.
Tel: 6-76-46-00
Telex: 17-74-507 HEWPACK MEX
A,CH,CS,E,MS,P
Hewlett-Packard Mexicana, S.A.
de C.V.
Ave. Colonia del Valle 409
Col. del Valle
Municipio de Garza Garza
MONTERREY, Nuevo Leon
Tel: 78 42 41
Telex: 038 410
CH
ECISA
José Vasconcelos No. 218
Col. Condesa Deleg. Cuauhtémoc
MEXICO D.F. 06140
Tel: 553-1206
Telex: 17-72755 ECE ME
M

MOROCCO

Dolbeau
81 rue Karatchi
CASABLANCA
Tel: 3041-82, 3068-38
Telex: 23051, 22822
E
Gerep
2 rue d'Agadir
Boite Postale 156
CASABLANCA
Tel: 272093, 272095
Telex: 23 739
P

NETHERLANDS

Hewlett-Packard Nederland B.V.
Van Heuven Goedhartlaan 121
NL 1181KK AMSTELVEEN
P.O. Box 667
NL 1180 AR AMSTELVEEN
Tel: (020) 47-20-21
Telex: 13 216 HEPA NL
A,CH,CM,CS,E,MP,P
Hewlett-Packard Nederland B.V.
Bongerd 2
NL 2906VK CAPELLE A/D IJSSEL
P.O. Box 41
NL 2900AA CAPELLE A/D IJSSEL
Tel: (10) 51-64-44
Telex: 21261 HEPAC NL
A,CH,CS,E

Hewlett-Packard Nederland B.V.
Pastoor Petersstraat 134-136
NL 5612 LV EINDHOVEN
P.O. Box 2342
NL 5600 CH EINDHOVEN
Tel: (040) 326911
Telex: 51484 hepae nl
A,CH*,*,E,M

NEW ZEALAND

Hewlett-Packard (N.Z.) Ltd.
5 Owens Road
P.O. Box 26-189
Epsom, AUCKLAND
Tel: 687-159
Cable: HEWPACK Auckland
CH,CM,E,P*
Hewlett-Packard (N.Z.) Ltd.
4-12 Cruickshank Street
Kilbirnie, WELLINGTON 3
P.O. Box 9443
Courtenay Place, WELLINGTON 3
Tel: 877-199
Cable: HEWPACK Wellington
CH,CM,E,P
Northrop Instruments & Systems Ltd.
369 Khyber Pass Road
P.O. Box 8602
AUCKLAND
Tel: 794-091
Telex: 60605
A,M
Northrop Instruments & Systems Ltd.
110 Mandeville St.
P.O. Box 8388
CHRISTCHURCH
Tel: 486-928
Telex: 4203
A,M
Northrop Instruments & Systems Ltd.
Sturdee House
85-87 Ghuznee Street
P.O. Box 2406
WELLINGTON
Tel: 850-091
Telex: NZ 3380
A,M

NORTHERN IRELAND

See United Kingdom

NORWAY

Hewlett-Packard Norge A/S
Folke Bernadottes vei 50
P.O. Box 3558
N-5033 FYLLINGSDALEN (Bergen)
Tel: 0047/5/16 55 40
Telex: 16621 hpnas n
CH,CS,E,MS
Hewlett-Packard Norge A/S
Østerdalen 16-18
P.O. Box 34
N-1345 ØSTERÅS
Tel: 0047/2/17 11 80
Telex: 16621 hpnas n
A,CH,CM,CS,E,M,P

OMAN

Khimji Ramdas
P.O. Box 19
MUSCAT
Tel: 722225, 745601
Telex: 3289 BROKER MB MUSCAT
P
Suhail & Saud Bahwan
P.O. Box 169
MUSCAT
Tel: 734 201-3
Telex: 3274 BAHWAN MB

PAKISTAN

Mushko & Company Ltd.
1-B, Street 43
Sector F-8/1
ISLAMABAD
Tel: 51071
Cable: FEMUS Rawalpindi
A,E,M
Mushko & Company Ltd.
Oosman Chambers
Abdullah Haroon Road
KARACHI 0302
Tel: 524131, 524132
Telex: 2894 MUSKO PK
Cable: COOPERATOR Karachi
A,E,M,P*

PANAMA

Electrónico Balboa, S.A.
Calle Samuel Lewis, Ed. Alfa
Apartado 4929
PANAMA 5
Tel: 63-6613, 63-6748
Telex: 3483 ELECTRON PG
A,CM,E,M,P

PERU

Cía Electro Médica S.A.
Los Flamencos 145, San Isidro
Casilla 1030
LIMA 1
Tel: 41-4325, 41-3703
Telex: Pub. Booth 25306
CM,E,M,P

PHILIPPINES

The Online Advanced Systems Corporation
Rico House, Amorsolo Cor. Herrera
Street
Legaspi Village, Makati
P.O. Box 1510
Metro MANILA
Tel: 85-35-81, 85-34-91, 85-32-21
Telex: 3274 ONLINE
A,CH,CS,E,M
Electronic Specialists and Proponents
Inc.
690-B Epifanio de los Santos Avenue
Cubao, QUEZON CITY
P.O. Box 2649 Manila
Tel: 98-96-81, 98-96-82, 98-96-83
Telex: 40018, 42000 ITT GLOBE
MACKAY BOOTH
P

PORTUGAL

Mundinter
Intercambio Mundial de Comércio
S.A.R.L.
P.O. Box 2761
Av. Antonio Augusto de Aguiar 138
P-LISBON
Tel: (19) 53-21-31, 53-21-37
Telex: 16691 munter p
M
Soquimica
Av. da Liberdade, 220-2
1298 LISBOA Codex
Tel: 56 21 81/2/3
Telex: 13316 SABASA
P
Telectra-Empresa Técnica de
Equipamentos Eléctricos S.A.R.L.
Rua Rodrigo da Fonseca 103
P.O. Box 2531
P-LISBON 1
Tel: (19) 68-60-72
Telex: 12598
CH,CS,E,P

PUERTO RICO

Hewlett-Packard Puerto Rico
Ave. Muñoz Rivera #101
Esq. Calle Ochoa
HATO REY, Puerto Rico 00918
Tel: (809) 754-7800
Hewlett-Packard Puerto Rico
Calle 272 Edificio 203
Urb. Country Club
RIO PIEDRAS, Puerto Rico
P.O. Box 4407
CAROLINA, Puerto Rico 00628
Tel: (809) 762-7255
A,CH,CS

QATAR

Computeabia
P.O. Box 2750
DOHA
Tel: 883555
Telex: 4806 CHPARB
P
Eastern Technical Services
P.O. Box 4747
DOHA
Tel: 329 993
Telex: 4156 EASTEC DH
Nasser Trading & Contracting
P.O. Box 1563
DOHA
Tel: 22170, 23539
Telex: 4439 NASSER DH
M

SAUDI ARABIA

Modern Electronic Establishment
Hewlett-Packard Division
P.O. Box 22015
Thuobah
AL-KHOBAR
Tel: 895-1760, 895-1764
Telex: 671 106 HPMEEK SJ
Cable: ELECTA AL-KHOBAR
CH,CS,E,M
Modern Electronic Establishment
Hewlett-Packard Division
P.O. Box 1228
Redec Plaza, 6th Floor
JEDDAH
Tel: 644 38 48
Telex: 4027 12 FARNAS SJ
Cable: ELECTA JEDDAH
CH,CS,E,M
Modern Electronic Establishment
Hewlett-Packard Division
P.O. Box 22015
RIYADH
Tel: 491-97 15, 491-63 87
Telex: 202049 MEERYD SJ
CH,CS,E,M
Abdul Ghani El Ajou
P.O. Box 78
RIYADH
Tel: 40 41 717
Telex: 200 932 EL AJOU
P

SCOTLAND

See United Kingdom

SINGAPORE

Hewlett-Packard Singapore (Sales)
Pte. Ltd.
#08-00 Inchcape House
450-2 Alexandra Road
P.O. Box 58 Alexandra Rd. Post Office
SINGAPORE, 9115
Tel: 631788
Telex: HPSGSO RS 34209
Cable: HEWPACK, Singapore
A,CH,CS,E,MS,P



SALES & SUPPORT OFFICES

Arranged alphabetically by country

SINGAPORE (Cont'd)

Dynamar International Ltd.
Unit 05-11 Block 6
Kolam Ayer Industrial Estate
SINGAPORE 1334
Tel: 747-6188
Telex: RS 26283
CM

SOUTH AFRICA

Hewlett-Packard So Africa (Pty.) Ltd.
P.O. Box 120
Howard Place **CAPE PROVINCE 7450**
Pine Park Center, Forest Drive,
Pinelands
CAPE PROVINCE 7405
Tel: 53-7954
Telex: 57-20006
A,CH,CM,E,MS,P
Hewlett-Packard So Africa (Pty.) Ltd.
P.O. Box 37099
92 Overport Drive
DURBAN 4067
Tel: 28-4178, 28-4179, 28-4110
Telex: 6-22954
CH,CM

Hewlett-Packard So Africa (Pty.) Ltd.
6 Linton Arcade
511 Cape Road
Linton Grange
PORT ELIZABETH 6000
Tel: 041-302148
CH

Hewlett-Packard So Africa (Pty.) Ltd.
P.O.Box 33345
Glenstantia 0010 **TRANSVAAL**
1st Floor East
Constantia Park Ridge Shopping
Centre
Constantia Park
PRETORIA
Tel: 982043
Telex: 32163
CH,E

Hewlett-Packard So Africa (Pty.) Ltd.
Private Bag Wendywood
SANDTON 2144
Tel: 802-5111, 802-5125
Telex: 4-20877
Cable: HEWPACK Johannesburg
A,CH,CM,CS,E,MS,P

SPAIN

Hewlett-Packard Española S.A.
Calle Entenza, 321
E-BARCELONA 29
Tel: 322.24.51, 321.73.54
Telex: 52603 hpbee
A,CH,CS,E,MS,P
Hewlett-Packard Española S.A.
Calle San Vicente S/No
Edificio Albia II
E-BILBAO 1
Tel: 423.83.06
A,CH,E,MS

Hewlett-Packard Española S.A.
Ctra. de la Coruña, Km. 16, 400
Las Rozas
E-MADRID
Tel: (1) 637.00.11
CH,CS,M

Hewlett-Packard Española S.A.
Avda. S. Francisco Javier, S/No
Planta 10. Edificio Sevilla 2,
E-SEVILLA 5
Tel: 64.44.54
Telex: 72933
A,CS,MS,P

Hewlett-Packard Española S.A.
Calle Ramon Gordoillo, 1 (Entlo.3)
E-VALENCIA 10
Tel: 361-1354
CH,P

SWEDEN

Hewlett-Packard Sverige AB
Sunnanvagen 14K
S-22226 **LUND**
Tel: (046) 13-69-79
Telex: (854) 17886 (via Spånga
office)
CH

Hewlett-Packard Sverige AB
Östra Tullgatan 3
S-21128 **MALMÖ**
Tel: (040) 70270
Telex: (854) 17886 (via Spånga
office)

Hewlett-Packard Sverige AB
Västra Vintergatan 9
S-70344 **ÖREBRO**
Tel: (19) 10-48-80
Telex: (854) 17886 (via Spånga
office)
CH

Hewlett-Packard Sverige AB
Skalholtsgatan 9, Kista
Box 19
S-16393 **SPÅNGA**
Tel: (08) 750-2000
Telex: (854) 17886
Telefax: (08) 7527781
A,CH,CM,CS,E,MS,P
Hewlett-Packard Sverige AB
Frötallsgatan 30
S-42132 **VÄSTRA-FRÖLUNDA**
Tel: (031) 49-09-50
Telex: (854) 17886 (via Spånga
office)
CH,E,P

SWITZERLAND

Hewlett-Packard (Schweiz) AG
Clarastrasse 12
CH-4058 **BASEL**
Tel: (61) 33-59-20
A

Hewlett-Packard (Schweiz) AG
7, rue du Bois-du-Lan
Case Postale 365
CH-1217 **MEYRIN 2**
Tel: (0041) 22-83-11-11
Telex: 27333 HPAG CH
CH,CM,CS

Hewlett-Packard (Schweiz) AG
Allmend 2
CH-8967 **WIDEN**
Tel: (0041) 57 31 21 11
Telex: 53933 hpag ch
Cable: HPAG CH
A,CH,CM,CS,E,MS,P

SYRIA

General Electronic Inc.
Nuri Basha Ahnaf Ebn Kays Street
P.O. Box 5781
DAMASCUS
Tel: 33-24-87
Telex: 411 215
Cable: ELECTROBOR DAMASCUS
E

Middle East Electronics
P.O.Box 2308
Abu Rummaneh
DAMASCUS
Tel: 33 4 5 92
Telex: 411 304
M

TAIWAN

Hewlett-Packard Far East Ltd.
Kaohsiung Office
2/F 68-2, Chung Cheng 3rd Road
KAOSHIUNG
Tel: (07) 241-2318
CH,CS,E
Hewlett-Packard Far East Ltd.
Taiwan Branch
8th Floor
337 Fu Hsing North Road
TAIPEI

Tel: (02) 712-0404
Telex: 24439 HEWPACK
Cable: HEWPACK Taipei
A,CH,CM,CS,E,M,P
Ing Lih Trading Co.
3rd Floor, 7 Jen-Ai Road, Sec. 2
TAIPEI 100
Tel: (02) 3948191
Cable: INGLIH TAIPEI
A

THAILAND

Unimesa
30 Patpong Ave., Suriwong
BANGKOK 5
Tel: 235-5727
Telex: 84439 Simonco TH
Cable: UNIMESA Bangkok
A,CH,CS,E,M
Bangkok Business Equipment Ltd.
5/5-6 Dejo Road
BANGKOK
Tel: 234-8670, 234-8671
Telex: 87669-BEQUIPT TH
Cable: BUSIQUIPT Bangkok
P

TRINIDAD & TOBAGO

Caribbean Telecoms Ltd.
50/A Jerningham Avenue
P.O. Box 732
PORT-OF-SPAIN
Tel: 62-44213, 62-44214
Telex: 235,272 HUGCO WG
CM,E,M,P

TUNISIA

Tunisie Electronique
31 Avenue de la Liberté
TUNIS
Tel: 280-144
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Bridewell Place
LONDON EC4V 6BS
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Telex: 298163
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LONDON COLNEY
Herts. AL2 1HA, St. Albans
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Easthampstead, **WOKINGHAM**
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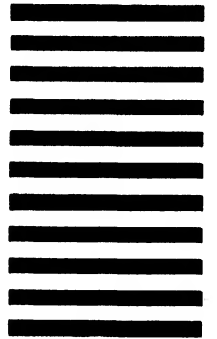
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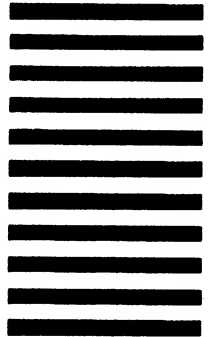
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